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Design and Characterization of RF-Power LDMOS Transistors

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Abstract
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In mobile communication new applications like wireless internet and mobile video have increased the demand of data-rates. Therefore, new more wideband systems are being implemented. Power amplifiers in the base-stations that simultaneously handle these wideband signals for many terminals (handhelds) need to be highly linear with a considerable band-width.

In the past decade LDMOS has been the dominating technology for use in these RF-power amplifiers. In this work LDMOS transistors possible to fabricate in a normal CMOS process have been optimized and analyzed for RF-power applications. Their non-linear behavior has been explored using load-pull measurements. The mechanisms of the non-linear input capacitance have been analyzed using 2D TCAD simulations. The investigation shows that the input capacitance is a large contributor to phase distortion in the transistor.

Computational load-pull TCAD methods have been developed for analysis of RF-power devices in high-efficiency operation. Methods have been developed for class-F with harmonic loading and for bias-modulation. Load-pull measurements with drain-bias modulation in a novel measurement setup have also been conducted. The investigation shows that the combination of computational load-pull of physical transistor structures and direct measurement evaluation with modified load-pull is a viable alternative for future design of RF-power devices. Simulations and measurements on the designed LDMOS shows a 10 to 15 % increase in drain efficiency in mid-power range both in simulations and measurements. The computational load-pull method has also been used to investigate the power capability of LDMOS transistors on SOI. This study indicates that either a low-resistivity or high-resistivity substrate should be used in manufacturing of RF-power LDMOS transistors on SOI to achieve optimum efficiency. Based on a proper substrate selection these devices exhibit a 10 % higher drain-efficiency mainly due to lower dissipated power in the devices.

Keywords: Power Amplifiers, LDMOS transistors, RF-power, IMD, Technology CAD, Load-Pull

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Success is not final, failure is not fatal:
it is the courage to continue that counts.

Winston Churchill

List of Papers

I "Novel BiCMOS Compatible, Short Channel LDMOS Technology for Medium Voltage RF & Power Applications," Andrej Litwin, Olof Bengtsson, and Jörgen Olsson, *IEEE MTT-S Int. Microwave Symp. Dig.,* pp. 35-38, 2002

II "Small Signal and Power Evaluation of Novel BiCMOS Compatible, Short Channel LDMOS Technology," Olof Bengtsson, Andrej Litwin, and Jörgen Olsson, *IEEE Trans. Microwave Theory Tech*., vol. 51, pp. 1052-1056, 2003

III "Investigation of the non-linear input capacitance in LDMOS transistors and its contribution to IMD and phase distortion," Olof Bengtsson, Lars Vestling, and Jörgen Olsson, *Solid State Electronics*, vol 52, no. 7, pp. 1024-1031, 2008

IV "A Method for Device Intermodulation Analysis from 2D, TCAD Simulations using a Time-domain Waveform Approach," Olof Bengtsson, and Lars Vestling, *Proceedings of the 36th EuMC*, pp. 169-171, 2006.

V "A Computational Load-Pull Method for TCAD Optimization of RF-Power Transistors in Bias-Modulation Applications," Olof Bengtsson, Lars Vestling, and Jörgen Olsson, Accepted to *EuMIC-2008*.

VI "A Computational Load-Pull Method with Harmonic Loading for High-Efficiency Investigations," Olof Bengtsson, Lars Vestling, and Jörgen Olsson, Submitted to *Solid State Electronics*

VII "Investigation of SOI-LDMOS for RF-power applications using Computational Load-Pull," Olof Bengtsson, Lars Vestling, and Jörgen Olsson, Submitted to *IEEE Transactions on Electron Devices*

VIII "A Novel Load-Pull Configuration for Envelope Tracking Applications,"
Olof Bengtsson, Lars Vestling, and Jörgen Olsson,
Submitted to *IEEE Trans. Microwave Theory Tech.*

The following papers are related to the work in this thesis but have not been included.

IX "Large Signal Characterization and Modelling of LDMOS-Transistors for RF-Power Applications,"
Olof Bengtsson, Anders Rydberg, Chen Qiang, Ted Johansson, Bengt Ahl, Kjell Wallin, and Francisco Purroy-Martin, *GHz'97*, Kista, Sweden, 1997.

X "RF-Power SiGe transistors for cellular base stations: base profile design,"
Ted Johansson, Olof Bengtsson, Anders Rydberg, and Edvard Nordlander, *RVK'99*, Karlskrona, Sweden, 1999.

XI "Optimization of high-voltage RF power SiGe transistors for cellular applications,"
Olof Bengtsson, Ted Johansson, Edvard Nordlander, and Anders Rydberg, *IEEE MIA-ME'99*, Novosibirsk, Russia, 1999

XII "On the Design of a Planar, Harmonic, Triplex-Filter for 3G, Load-Pull Measurement Applications,"
Patricia Castillo, Ebert San-Roman, and Olof Bengtsson, *RFMTC-07*, Gävle, Sweden, 2007

XIII "A Computational Load-Pull Investigation of Harmonic Loading effects on AM-PM conversion,"
Olof Bengtsson, Lars Vestling, and Jörgen Olsson, *GHz2008*, Gothenburg, Sweden, 2008

XIV "High Efficiency using Optimized SOI Substrates,"
Lars Vestling, Olof Bengtsson, and Jörgen Olsson, *GHz2008*, Gothenburg, Sweden, 2008

Contents

Abbreviations

2D	Two Dimensional
3D	Three Dimensional
ACLR	Adjacent Channel Leakage Ratio
AM	Amplitude Modulation
ATS	Automated Tuner System
AWG	Arbitrary Waveform Generator
BiCMOS	Bipolar and Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
CLP	Computational Load-Pull
CMOS	Complementary Metal Oxide Semiconductor
CW	Continuous Wave
DPD	Digital Pre-Distortion
DUT	Device Under Test
EER	Envelope Elimination and Restoration
ET	Envelope Tracking
FEM	Finite Element Method
FFT	Fast Fourier Transform
GaAs	Gallium-Arsenide
GaN	Gallium-Nitride
GSM	Global System for Mobile communications
HB	Harmonic Balance
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HFET	Heterojunction Field Effect Transistor
HFSS	High Frequency Structure Simulator
IM	Intermodulation
IMD	Intermodulation Distortion

LDMOS	Lateral Double-Diffused Metal Oxide Semiconductor
LF	Low Frequency
LNA	Low Noise Amplifier
LRM	Line Reflect Match
LSNA	Large-Signal Network Analyzer
LSTD	Large-Signal Time-Domain
LTE	Local Truncation Error
MCPA	Multi Carrier Power Amplifier
MESFET	Metal Semiconductor Field Effect Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MTA	Microwave Transition Analyzer
PA	Power Amplifier
PAE	Power Added Efficiency
PM	Phase Modulation
RADAR	Radio Detection And Ranging
RF	Radio Frequency range, Telecommunication and WLAN frequencies, prev. <1 GHz
RFIC	Radio Frequency Integrated Circuit
SCPA	Single Carrier Power Amplifier
Si	Silicon
SiC	Silicon-Carbide
SiGe	Silicon-Germanium
SOI	Silicon On Insulator
SOLT	Short Open Load Through
TCAD	Technology Computer Aided Design
TRL	Through Reflect Line
TRX	Transceiver Unit
UHF	Ultra-High Frequency, 300 MHz to 3 GHz
UMTS	Universal Mobile Telecommunications System
VLSI	Very Large Scale Integration
VNA	Vector Network Analyzer
WCDMA	Wideband Code Division Multiple Access
WiMAX	Worldwide Interoperability for Microwave Access
VSWR	Voltage Standing Wave Ratio

Selected List of Symbols

BV	Breakdown Voltage
C_{OX}	Oxide Capacitance
d_{OX}	Oxide Thickness
f_{MAX}	Maximum Oscillation Frequency, MAG cutoff frequency
f_T	Transition Frequency, Current gain cutoff frequency
G	Gain (Transducer Gain)
g_m	Transconductance
IQ	In-Phase and Quadrature Component
I_{DC}	DC Current Supply
I_{DMAX}	Maximum Drain Current
I_{DQ}	Quiescent Drain Current
L_{CH}	Channel Length
L_{D1}	First Drift-Region Length
L_{D2}	Second Drift-Region Length
P_{AVS}	Power Available from Source
P_1	Power at Fundamental Component
P_{1dB}	1 dB Compression Point
P_D	Dissipated Power
P_{DC}	DC Power
P_{IN}	Input Power
P_L	Power Delivered to Load
P_{OUT}	Output Power
P_{RF}	Power at Radio Frequency
Q	Quality Factor
v_D	Time-varying Drain Voltage
V_D	Drain Voltage
V_{DC}	DC Voltage Supply

v_G	Time-varying Gate Voltage
V_G	Gate Voltage
V_S	Supply Voltage
Z_0	Characteristic Impedance
Z_L	Load Impedance
Z_S	Source Impedance
E	Electrical Field
T	Temperature
T_M	Measurement Temperature
$\Delta\phi$	Phase Difference
ε_{OX}	Oxide Permittivity
η_D	Drain Efficiency
ϕ	Phase
Γ	Reflection Coefficient

1. Preface

This thesis is about design and evaluation of radio frequency, RF, power transistors for power amplifiers for modern telecommunication applications. For these applications silicon lateral double-diffused metal oxide semiconductors, LDMOS, has been the dominating technology the past decade. It is today a mature cost-effective technology that will be a feasible alternative also for future generations of telecommunication systems above 3.5 GHz. Modern applications with increased need of bandwidth have placed high demands on power amplifiers, especially regarding linearity. Meeting these requirements overall system efficiency is low. On system level different directions for improvements have been identified. For medium power, subsystem integration is one possibility. With integrated power-devices, power amplifiers and linearization techniques might be possible to integrate in single chip solutions.

The LDMOS transistor in this work was designed to enable the possibility of making LDMOS transistors as part of an integrated circuit in a normal bipolar and complemetary-metal-oxid-seminconductor, BiCMOS, process. With the combination of the power performance of the LDMOS and the vast amount of library components available in CMOS, full amplifiers can be designed as inexpensive radio frequency integrated circuits, RFICs.

For higher power there are many options. Linear mode power amplifiers are now reaching their theoretical limit of efficiency. Therefore old methods for efficiency enhancement like envelope-tracking and more efficient switch-mode solutions are now considered. Improving amplifier performance is much related to improving the RF-power transistors in the amplifier. The main characteristics of the amplifier come from the limitations of the RF-power transistors. RF-Power transistors are designed using simulations of fabrication and device performance based on the physical structure of the device.

The second part of this work deals with methods to improve large-signal simulations of physical structures of RF-power transistors for new high-efficiency modes of operation. It also deals with methods to characterize them under the same conditions. The aim of this work has been to enable large-signal pre-fabrication device analysis, both for device optimization in normal operation and for new more demanding high-efficiency applications. These applications include envelope-tracking and high efficiency class-F amplifiers. It is expected that these simulation and

evaluation methods will reduce the need for tedious device modeling and time consuming demo-design in the device design process.

Chapter 2 gives a brief introduction to the subject and the motivation of the work. Some basic power amplifier specifications are explained and the system level impact on device development is discussed. It also includes a short introduction to TCAD.

Chapter 3 briefly covers the design and evaluation of the LDMOS for BiCMOS processing. Results from the evaluation of the concept are also given. The originally simulated and fabricated LDMOS describer in this part has been used extensively in this work to illustrate the methods presented.

In chapter 4 large-signal load-pull simulations and characterization is explained. Large-signal computational load-pull simulations of physical device structures are described in detail, especially the large-signal time-domain methods used in this work. Load-Pull measurement-systems are also explored. The final part of the chapter covers the simulated and measured results.

Finally some concluding remarks are made about this work in general and the future possibilities with it.

2. Introduction

The function of the metal oxide semiconductor field effect transistor, MOSFET, was first proposed in a patent application filed on March 28, 1928, by J. E. Lilienfeld [1]. It would take until the mid 60s before fabrication techniques reached a standard high enough to fabricate the suggested device. Meanwhile the bipolar junction transistor, BJT, was proposed, designed and fabricated at Bell labs by Bardeen, Brattain and Shockley in the 1940s [2], [3]. Initially a laboratory point contact device but refined processing methods soon made mass-production possible. The first bipolar transistors were made of germanium but in the early 1960s silicon devices fast replaced the germanium devices much due to the ease of making silicondioxide, SiO_2, layers for passivation [4]. In 1958 several transistors were combined on a chip and the first bipolar integrated circuit was designed. In 1960 processing had improved and the first silicon MOSFET was designed and fabricated [5]. Just a few years later in 1963, complementary MOS or CMOS was presented laying the foundation for the coming integrated CMOS circuit [6]. Today these very large scale integrated circuits, VLSI, are fabricated on 200 mm wafers in complex BiCMOS processes enabling the design of both bipolar and CMOS on the same wafer. The historical goal and driving force is and has always been to minimize the power consumption and increase the speed [7].

2.1 RF-Power History

The first transistors for operation above 1 GHz were germanium mesa devices from 1958-59, [4]. In the mid 1960s silicon had replaced germanium in most applications except for the extreme high frequency operation where the higher mobility of germanium made it favorable in those applications. For power devices germanium was unsuitable due to the narrower bandgap rendering it intrinsic at quite low junction temperatures [8]. Although the MOSFET soon became dominant for low frequency applications and CMOS for digital circuits, silicon bipolar continued to be mainstream for power applications at ultra high frequency, UHF, (300 MHz to 3 GHz) until the late 1980s [9]. In power amplifiers for telecommunication in the higher UHF bands Si-BJT transistors were not replaced until the lateral double-diffused metal oxide semiconductor, LDMOS, entered the scene in 1996. New

modulation and multiplexing techniques in modern telecom systems had placed higher demands on the power amplifiers, PAs, in the systems. The superior linearity in LDMOS transistors immediately made them the main choice. The telecommunication industry adopted the new technology fast despite initial problems with hot carrier injection [10], [11]. For more than a decade LDMOS has been the dominating technology for RF-power amplifiers. It is a mature technology that has seen great improvements over the years. With improved efficiency being the main goal Si-LDMOS is now reaching its limit in performance [12]. Even so recent work implies that it will be a competitive candidate even for WiMAX systems above 3.5 GHz [13]. Due to the rather simple processing and special design silicon RF-power transistors were traditionally made in separate processes sometimes in older foundries. This continued also after the introduction of the LDMOS and is still valid today mainly because the processing does not require state of the art lithography.

Work at higher frequencies in the microwave bands was mainly military and vast amount of money was spent on developing processing and devices in gallium-arsenide, GaAs. This created a mature but expensive technology available also for commercial applications in the late 1980s. Today this technology is cost competitive and available both for high-speed integrated circuits and discrete microwave power transistors. In recent years processing development has also made it possible to fabricate RF-power devices in new compound-material semiconductors like silicon-carbide, SiC, and gallium-nitride, GaN. Due to their material properties they are expected to have superior performance for high-power microwave devices which has also been shown in recent work [14]. Much research is now done in this field and some products are already on the market but for mainstream applications they are not yet cost competitive even if the physical properties are promising. With higher breakdown field, smaller devices with less capacitance for the same output power are possible, table 2.1.

	Ge	Si	GaAs	SiC	GaN
Mobility (cm^2/Vs)	3900	1450	8500	1140	1250
Breakdown field (V/μm)	10	30	60	300	500

Table 2.1. Physical properties for semiconductor material proposed for RF-power.

With improved material quality and processing it is likely that future PA designers will have a greater choice of technology to use. Depending on application and architecture one technology will be chosen before another. LDMOS transistors are mainstream today for PA-designers and will continue to be so for many years much due to the mature inexpensive technology.

2.2 Some PA Specifications

The RF-power transistor is the main component in the power amplifier. When power performance is characterized for an RF-power transistor it is done by evaluating it as part of an amplifier. This is either done using a build demo-design amplifier or in a measurements system that together with the transistor emulates an amplifier (load-pull). Since the properties are measured in a demo-design or measurement system emulating an amplifier they are only valid under the conditions generated in that environment (see chapter 4). Some specifications relate to their analog properties like gain, efficiency and two-tone intermodulation distortion, IMD. For device designers these analog properties constitute the mainly used specifications for technology improvement. They are easy to correlate to the mechanisms and the design of the component. If they are measured under load-pull conditions they provide a general basic technology evaluation unlimited by design constraints.

Modern RF-power components are usually designed for a certain telecom system with specific signal characteristics. It is therefore sometimes of interest to give system unique specifications. Fundamental specifications like gain and efficiency are then also measured for system specific wideband signals. For these signals additional specifications relate to the non-linearities of the amplifier. Most important is spectral regrowth which specifies how much energy is spilling over from the wanted radio channel into adjacent channels [15]. Properties deduced for one type of digitally modulated signal are generally not convertible to a signal with different characteristics. The specifications are unique with regards to e.g. signal bandwidth and crest factor.

Increasingly important for power amplifiers in wideband systems are the so called memory-effects. Mechanisms with different time-constants, mainly related to the biasing system and heat-generation cause spectral regrowth and sideband asymmetries. This can be observed both for analog signals as IMD asymmetry and for digitally modulated signals as regrowth asymmetry. Much work on memory-effects is related to behavioral modeling of power amplifiers [16]. These models are normally based on measurement systems for digital base-band characterization [17]. Being systems for in-band measurements of full amplifiers with fixed matching the properties found are of limited use for transistor development. For device designers they merely provide figure of merits for technology comparison. This may change in a near future when these systems merge with traditional load-pull. The general amplifier (including the RF-power transistor) setup is shown in figure 2.1.

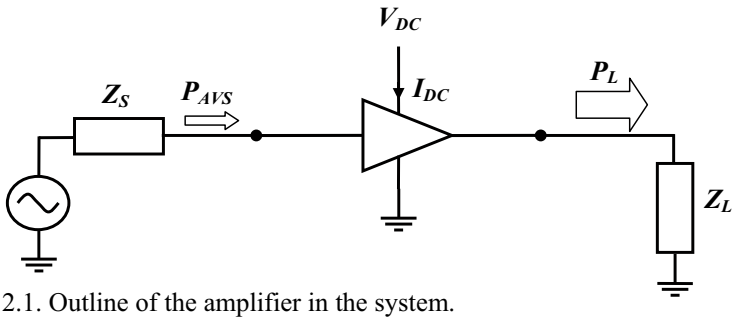

Figure 2.1. Outline of the amplifier in the system.

P_{AVS} is the power available form source with source impedance Z_S, P_L is the power delivered to the load with load impedance Z_L. In a normal telecom system Z_L and Z_S are equal to the characteristic impedance 50 Ω. V_{DC} is the voltage supply to the amplifier (normally 28 V for a base-station PAs) and I_{DC} is the DC current. For matched input the input power to the amplifier, P_{IN}, is equal to the power available from the source, P_{AVS}. For a matched load the output power of the amplifier, P_{OUT}, is equal to the power delivered to the load, P_L.

2.2.1 Gain

There are many definitions of gain. When just referred to as gain it normally implies the transducer gain which is the relationship between the continuous wave, CW, power delivered to the load and the power available from the source (2.1).

$$G = \frac{P_L}{P_{AVS}} \tag{2.1}$$

For matched amplifier conditions they become the more intuitive (2.2)

$$G = \frac{P_{OUT}}{P_{IN}} \tag{2.2}$$

In the frequency domain the gain can be found from the increase in power at the fundamental frequency as show in figure 2.2.

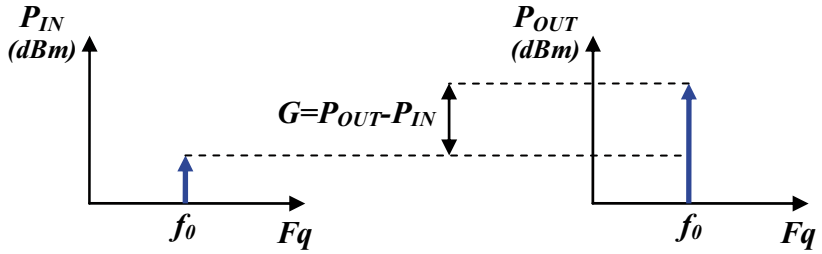

Figure 2.2. Gain observed in the frequency spectrum.

The gain should be as constant as possible for a large span of input power. For modulated signals the gain can be measured as power increase within the channel. Normal value for a modern 100W RF-power Si-LDMOS is about 16-20 dB at 2 GHz [12].

2.2.2 Power Compression, AM to AM

The main function of the power amplifier is to increase the output power. Its ability to do that is usually specified as the output power at the 1 dB compression point, P_{1dB}, under continuous wave conditions. This point indicates when the output power has reached a power level where the signal due to compression is deviating 1 dB from its extrapolated linear response as shown in figure 2.3.

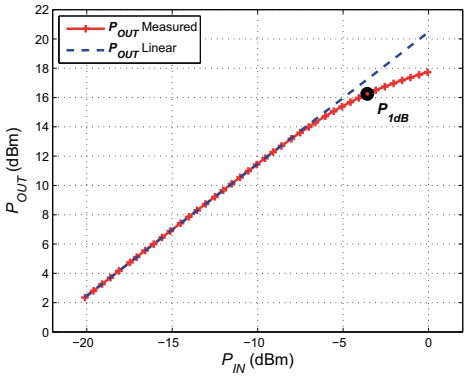

Figure 2.3. Output power versus input power with 1 dB compression point noted.

Power compression is usually measured using a vector network analyzer, VNA, with a linear power sweep. It is sometimes referred to as the AM to AM distortion (AM for amplitude modulation). Reaching compression means that power will be generated at harmonics of the fundamental frequency and the frequency spectrum becomes as in figure 2.4.

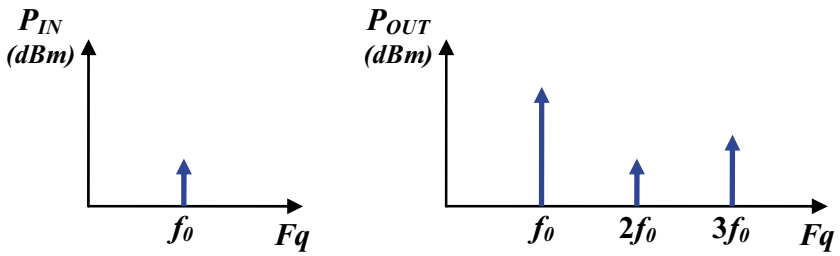

Figure 2.4. Compression observed in the frequency spectrum.

2.2.3 Phase Distortion, AM to PM

When the transistor reaches compression (sometimes before) the phase response of the amplifier also starts to deviate. Measuring the phase of the gain of the fundamental frequency (S21) with increasing input power using a VNA gives the AM to PM conversion (PM for phase modulation).

2.2.4 Efficiency

The efficiency parameters relate to the amplifiers ability to convert DC-power to RF-power. Only the power of the fundamental component is of interest for telecom applications. There are two efficiency definitions widely in use. The drain-efficiency (or only efficiency) and the power-added efficiency.

Drain-Efficiency
The drain-efficiency is defined as the relationship between the output power at the fundamental frequency and the supplied DC-power (2.3), [15].

$$\eta_D = \frac{P_{OUT}(f_0)}{P_{DC}} = \frac{P_{OUT}(f_0)}{V_{DC} I_{DC}} \qquad (2.3)$$

Power-Added Efficiency
The power-added efficiency, PAE, also considers the input power (2.4), [15].

$$PAE = \frac{P_{OUT}(f_0) - P_{IN}(f_0)}{P_{DC}} \qquad (2.4)$$

For a high gain devices PAE and drain-efficiency reaches almost the same values. The main factor affecting efficiency is the biasing of the transistor in the amplifier. The theoretical limits of efficiency increase with reduced transistor conduction angle. From linear class-A (50 %), through reduced conduction angle class-AB to class-B (78.5 %) to pulsed mode class-C reaching 100 % efficiency for 0 ° conduction angle [18]. There is however always a trade-off, high efficiency usually means more non-linearities.

2.2.5 Intermodulation Distortion

When the amplifier is working in compression it starts to generate power at harmonic frequencies. Normally these unwanted signals can be filtered out. For closely spaced signals non-linearities create mixing-products close to the carrier. These are referred to as intermodulation distortion, IMD.

Two-tone Intermodulation Distortion

Multi-tone narrow spaced CW signals give rise to mixing products close to the carries difficult to remove with filters [15]. They are typically measured using two-tone test configurations. A typical two-tone frequency spectrum is shown in 2.5.

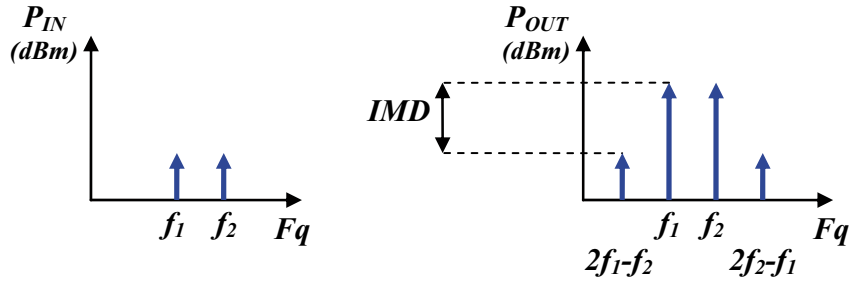

Figure 2.5. Frequency spectrum of third order intermodulation distortion.

Higher order IMD is found further from the carriers. IMD is measured relative to carrier in dB or as absolute power in dBm. Typical results from these measurements are sweeps of IMD versus input power and/or output power. An example is shown in figure 2.6.

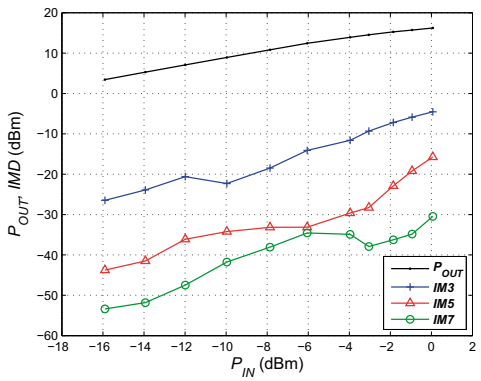

Figure 2.6. Two-tone IMD measurement of LDMOS transistor in class-AB.

In recent years it has been noted that the IMD products created in the upper frequency bands and in the lower frequency bands can have somewhat different amplitude. This is referred to as sideband asymmetries. This is illustrated in figure 2.7

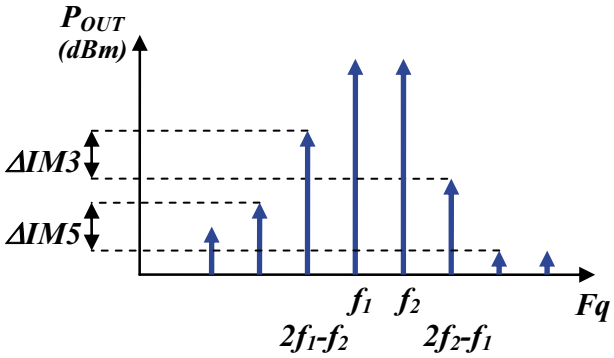

Figure 2.7. Frequency spectrum of intermodulation distortion with sideband asymmetries.

Investigations have shown that these asymmetries arise from memory-effects. The level of asymmetry depends upon tone-spacing. Measuring these asymmetries is sometimes used as a method of characterizing the memory-effects [19].

Adjacent Channel Leakage

For digitally modulated signals the signal power is spread in a channel in the spectrum and not located in single tones. Amplitude and phase distortion combine with intermodulation in the band and memory-effects. Together all non-linearities create an overall spread of energy and spectral regrowth in the adjacent channels as shown in figure 2.9.

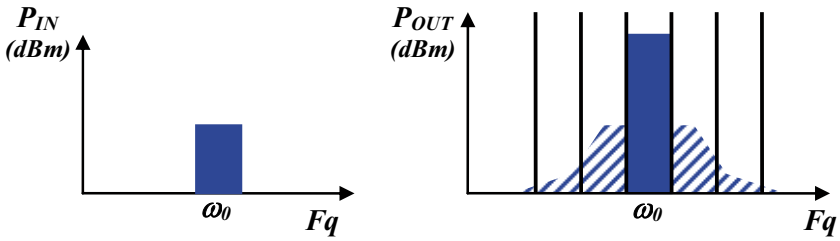

Figure 2.9. Frequency spectrum of digitally modulated wideband signal illustrating spectral regrowth in adjacent channels.

The amount of power in the adjacent channels is measured relative to the carrier in the wanted channel or as an absolute power in the adjacent channel. It is referred to as the adjacent channel leakage ratio, ACLR. It is measured with specific instrumentation settings related to the unique radio system, for example specific radio channel filters [20].

2.3 System Aspects on Transistor Development

When the first RF-power components were designed the applications they were intended for were usually narrowband high power applications like radar or broadcasting. High power and high efficiency were the most important figure of merits. For the past two decades the driving force has instead been the telecommunication industry. With increasingly complex modulation and multiplexing creating wideband signals with high peak to average ratios the linearity of the devices has become increasingly important. The need to reduce cost and simplify transceiver architecture has also placed additional demands on the devices. The introduction of multi carrier power amplifiers, MCPAs, have further increased the PA bandwidth and peak to average it needs to handle. To meet the system demands linearization circuitry external to the amplifier has been implemented. Overall system efficiency is low. This does not only imply high energy costs but also high cost for infrastructure and maintenance of cooling systems. Today much work is done in order to increase system efficiency. Switch-mode amplifiers are considered a viable alternative but they are inherently non-linear and need additional solutions to provide linear amplification. An intermediate step may be to boost the efficiency of linear amplifiers by use of envelope-tracking. From a device perspective switch-mode and envelope-tracking create fundamentally different working conditions than present linear-mode operation. The transistors are today not optimized for these applications and much work remains in this field.

2.3.1 PA Architecture

The purpose of the power amplifier in a base-station for mobile telephony is to increase the power of the transmitted signal from the transceiver to enable signal strength for full coverage of the mobile cell area as shown in figure 2.10. The highest transmitter power-class for a GSM 900 base-station has an output power of 320-640 W [21].

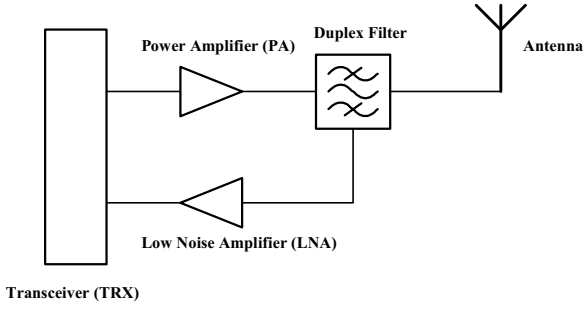

Figure 2.10. Outline of a typical base-station for mobile communication.

With the introduction of digital modulation in the second generation of mobile telephony it became increasingly important that the amplification was done without distorting the signal since any distortion in phase or amplitude might cause corruption of symbols with erroneous data as a consequence. The solution was to use more linear operation and combine it with external linearization like feed-forward or pre-distortion as shown in figure 2.11, [22]. With linearization system specifications could be met but overall system efficiency was low. This created more complex base-station systems with considerable cost for cooling of the system to remove energy lost as heat.

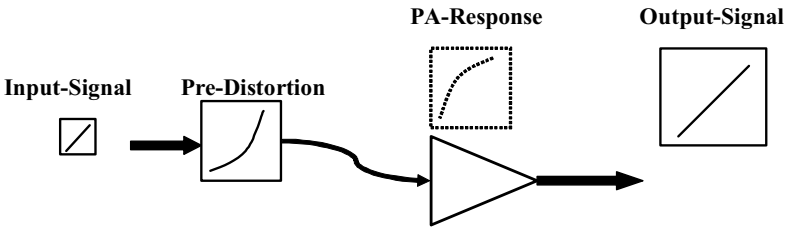

Figure 2.11. Outline of power amplifier with pre-distortion.

Early base-stations were typically using single-carrier power amplifiers, SCPAs, i.e. one PA for every transmitter and carrier as shown in figure 2.12. The architecture of a base-station using SCPAs is quite complex and involves high-power combining [22].

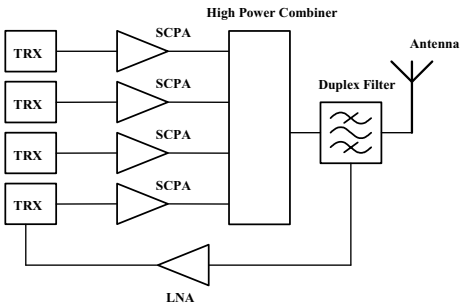

Figure 2.12. Base-station transceiver system using single-carrier power amplifiers.

Even though the losses in the combiner are low the amount of power combined causes severe heating. Using multiple PAs also makes the system expensive. To overcome these problems many modern systems instead use multi-carrier power amplifiers, MCPAs, where several low power signals from the transceivers are combined and feed into the same amplifier as shown in figure 2.13, [22].

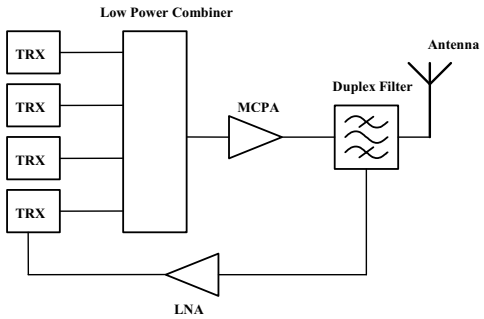

Figure 2.13. Base-station transceiver system using multi-carrier power amplifiers.

The combination of several carriers in the amplifiers have made it necessary to design them for much higher peak to average signals due to the possible statistical combination of envelopes in the different carriers. Even with the use of advanced linearization techniques it is often necessary to operate the amplifier in backed-off conditions far from the compression level [15], [22]. The overall system efficiency is therefore quite low. A typical UMTS-WCDMA base-station with four carriers (MCPA) and an output power of 60 W has a typical efficiency of 8.8%, [23].

2.3.2 Efficiency Enhancement

Today much effort is spent on increasing the overall system efficiency and the key issue is to raise the efficiency of the power amplifiers. In order to do this, old amplifier architectures for high efficiency operation like envelope-tracking, ET, and envelope elimination and restoration, EER, (Kahn amplifiers) are now considered [24]-[26]. These technologies have been available in low-voltage PAs for handhelds for a number of years but are now also implemented for high-voltage PAs for base-stations.

Envelope-Tracking

The principle of envelope-tracking is to always let the amplifier work in high-efficiency compression by adjusting the bias, i.e. the gate or drain voltage. A schematic outline of an envelope tracking system is shown in figure 2.14.

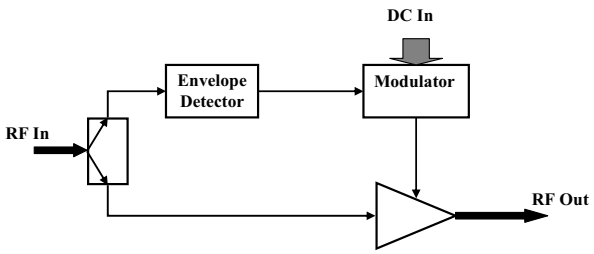

Figure 2.14. Schematic outline of envelope-tracking system with bias-modulation.

The modulated RF signal is split in two paths. In one path the envelope is detected. The envelope signal is then used to modulate the supply for the RF-amplifier in the second path. Bias-modulation like this is well suited to boost the efficiency for linear-mode class-AB amplifiers in mid-power range below compression but can also be used for switch-mode amplifiers [25].

Switch-Mode Amplifiers

Traditionally class-AB has been used for PA design in telecommunication applications. Class-AB has provided a fair tradeoff between linearity and efficiency [15], [18]. There is a theoretical limit of 78.5 % drain efficiency based on a signal level close to compression. For modern high peak to average signals the amplifier is forced to work under backed-off conditions. Then class-AB simply does not provide an efficient solution. For increased efficiency switched-mode amplifiers class-D (with D^{-1}), E and F (with F^{-1}) are now considered [18]. The switch-mode amplifiers basically amplify a constant envelope signal as shown in figure 2.15.

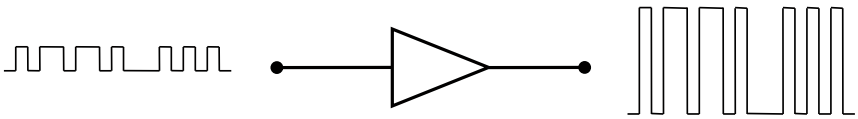

Figure 2.15. Switch-mode amplifier with constant envelope signal.

The switch-mode amplifier can maintain the phase-modulation in the signal but is normally only used for constant envelope signals. Class-E and class-F (with class-F^{-1}) have some linear gain and can maintain amplitude modulation but the high efficiency is reached close to compression. Switch mode amplifiers are today implemented in both compound materials and traditional Si-LDMOS technology. A summary of state of the art achievements the past two years is shown in table 2.2.

Class	Material	Technology	f (GHz)	P_{OUT} (dBm)	G (dB)	η_D (%)	Ref.	Year
D^{-1}	Si	LDMOS	1	43	15.1	71	[27]	2006
D^{-1}	GaN	MESFET	0.9	48.3	-	78	[28]	2007
E	Si	LDMOS	2.14	39.8	13.8	65.2	[29]	2007
E	SiC	MESFET	2.14	40.3	10.3	79.7	[29]	2007
E	GaN	HEMT	2.14	43	13	73.7	[29]	2007
F^{-1}	Si	LDMOS	1	41.2	16	73.7	[30]	2006
F	GaN	HEMT	2	42.2	13	91	[31]	2007

Table 2.2 State of the art performance for switched-mode power amplifiers

Since the amplifiers are far from linear the amplitude modulation needs to be restored for varying envelope signals. There are mainly two ways of doing this: load-modulation where the load impedance is altered based on envelope information [32] and bias-modulation which is used in ET and EER systems.

Envelope Elimination and Restoration

If a limiter and a switched mode amplifier are used in the RF path the envelope tracking system becomes an envelope elimination and restoration system. A schematic outline is shown in figure 2.16.

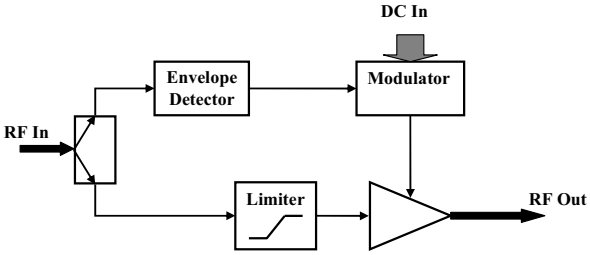

Figure 2.16. Schematic outline of envelope elimination and restoration system.

A more modern ET/EER transceiver architecture would get the envelope information directly from the base-band as shown in figure 2.17.

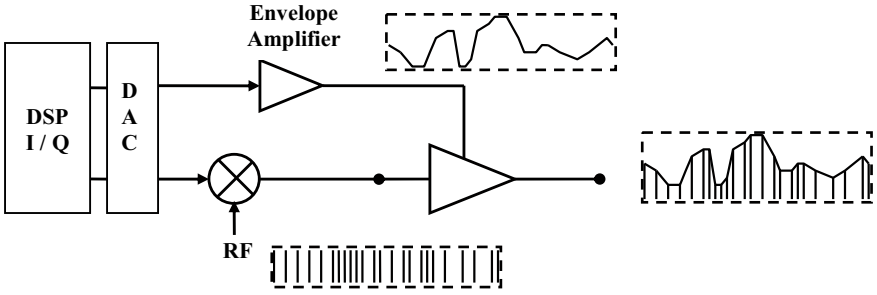

Figure 2.17. Schematic outline of modern transceiver system with bias-modulation from envelope amplifier.

The main concerns related to ET and EER systems are the limited efficiency of the wideband drain-bias modulation circuitry and possible distortion introduced by the efficiency enhancement system [33]. With an accurate PA model, digital pre-distortion, DPD, can be used to create an overall linearity that meets modern system requirements. For LDMOS technology an overall PAE of 40.4 % has been reported for a 27 W single-carrier WCDMA amplifiers utilizing ET together with DPD [34]. GaN HFET technology has shown even higher values at 50.7 % PAE with 37 W output power [35]. These are promising results compared to the 8.8 % in products today [23]!

2.4 Technology CAD

Technology CAD or TCAD is a physics based simulation tool used for pre-fabrication process and device optimization. In TCAD all simulations are conducted on physics-based finite element (FEM) structures defined by their material-composition and charge-distribution. The finite elements in the simulations are defined by a grid or mesh. The structures are "fabricated" in process simulations by simulating each process step in the process flow [36]. Every process-step like oxidation or implantation has its own model that describes the physics or chemistry in the process-step. The model parameters are controlled to best fit the process-flow that will be used in the true fabrication and step by step fabrication of the devices is simulated.

For simulation of electrical behavior commercial tools like Atlas from Silvaco and Dessis from Synopsys readily provide DC, small-signal and transient electrical solutions for 1D-3D structures. The ability to store solutions during electrical simulations enables the study of transport and breakdown mechanisms in the structure. Electro-thermal models can be used to include self-heating. Since TCAD is based on finite element methods it can be time consuming for good accuracy but with improved computer performance and computation algorithms even large signal simulations for RF-power devices are now feasible on ordinary personal computers (see chapter 4.1).

2.4.1 Device Simulations

When the structure is completed in the process simulator it is evaluated with regard to its electrical characteristics in a device simulator. This is done by numerically solving Poisson's equation on differential form (time domain) for the full structure of finite elements under different boundary value conditions like gate and drain voltage [37].

Recombination, mobility models and other parameters have to be defined. They are usually found from measurements of previously fabricated devices from the same process flow. Good agreement with fabricated devices is possible with careful tuning of the model parameters. Fair agreement is usually sufficient and more time efficient for comparative studies of different structures and for qualitative investigations of different mechanisms.

The Lombardi inversion-layer mobility-model was used in the simulations in this work [38]. In this semi-empirical model the mobility is considered to be the sum of three terms, the carrier mobility limited by scattering with surface acoustic phonons, the bulk silicon mobility, and the mobility limited by surface roughness scattering.

Due to the high transverse field in the channel region combined with the bulk properties of the drift region this model have shown to be the most accurate one for LDMOS transistors [39].

2.4.2 Simulation Interface

RF-power transistors are designed to be the final link in the amplification chain. As such they must produce a considerable amount of power and therefore have a considerable size. A layout that was already used in the 1960s for bipolar transistors and is still in use for LDMOS is the interdigitated layout shown in figure 2.18, [40].

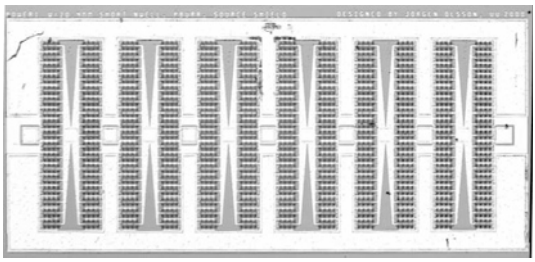

Figure 2.18. Transistor die with interdigitated structure for RF-power transistor.

Each die can contain a large number of gate and drain fingers and can be considered as numerous amount of transistors connected in parallel. Some fingers are further away from the common feed pads and the mere size of the die creates distributed parasitic effects hard to model [41]. For really high output power multiple dies can be connected in parallel within the same transistor package. The drain and gate contacts on the dies are bonded to the package leads with bond-wires. Source is connected thorough the substrate to the bottom flange which also works as heat-remover. The rows of bond-wires introduce inductance and the large metal leads they are connected to capacitance. It is a linear but complex system with self- and mutual- inductance and capacitance, all referred to as package parasitics. They are best simulated in a full 3D electromagnetic simulator like HFSS where a physical model can be made of the package and bond-wire geometry [42]-[44]. Due to the large number of transistors in parallel the impedances get very low and internal matching is often used. Internal chip capacitors together with the inductance from the bond-wires transform the impedances to higher more practical design values at the leads of the transistor package.

The die part of the transistor can be simulated in 3D TCAD but it is very time consuming. 3D TCAD is only used when necessary for example in the study of 3D effects like third dimension breakdown or distributed parasitics. Since TCAD equations are solved for every finite element the simulation-time grows exponentially with the number of elements in the structure. For an RF-power transistor with numerous fingers it would be impractical to

accurately simulate a full die or even more than a couple of fingers on a normal modern computer. This is however not a great limitation. The amplification and mechanisms associated with it can be found in the 2D intrinsic device. Using a 2D structure a more accurate simulation can be done of the actual transistor region since smaller finite elements (finer grid) can be simulated in the same amount of time due to a reduce total number of elements in a 2D simulation. In 2D, structures can also be compared under similar conditions intrinsic to any package and third dimension parasitics. The TCAD simulations in this work were all conducted in 2D.

2.5 Summary

The increasing market and decreasing margins for digital base-station power amplifiers in personal communication systems requires low-cost ease-of-use technology that can provide high power and good linearity performance. LDMOS was introduced in 1996 and has since then replaced bipolar in RF-power applications mainly due to its high gain and excellent back-off linearity [45]. Today LDMOS is the leading technology for high power base-station amplifiers and will be a viable alternative also for systems above 3.5 GHz [13]. New compound semiconductors have shown excellent performance and will find their marked in specific applications. For high-efficiency switch-mode amplifiers, ET and EER systems with bias-modulation are used to restore the amplitude modulation. These methods force the RF-power transistors to operate under much different conditions than the linear-mode constant voltage supply they were optimized for. For LDMOS transistors the voltage dependency of the output capacitance poses a problem for bias-modulated applications. At low supply voltage the change of output capacitance causes the optimum load-impedance to change. For constant load-impedance matching networks (normal amplifiers) the result becomes a mismatch with severe amplifier gain-decrease with reduced supply voltage.

TCAD is a versatile tool for process simulation and electrical evaluation of physical device structures. Good agreement with fabricated devices is possible with careful tuning of the model parameters. 2D simulations provide an interface where the fundamental mechanisms can be studied directly, intrinsic to third-dimension and package parasitics

The work conducted in this thesis makes it possible to study physical RF-power transistor structures under high-efficiency operation prior to fabrication. With the simulation methods developed in TCAD it will be possible to optimize and evaluate the RF-transistors under true operating conditions in these high-efficiency applications. Today this optimization is normally done based on extracted models from fabricated devices or based on full amplifier characterization under varying bias conditions [46].

3. The Designed LDMOS Transistor

Most of the work in this thesis was conducted on a device developed within the Linear Integrated Multicarrier Power Amplifier project or in short LIMPA project at Ericsson Microelectronics. It was aimed at designing a medium to high voltage RF LDMOS module in a normal CMOS process using an angular implant of the p-well. The method of implementing the LDMOS in a Bi-CMOS process described herein was patented by Söderbärg et al. for Telefonaktiebolaget LM Ericsson, Stockholm in 2004 [47]. The succeeding sections relate to some of the aspects of the simulations conducted in the design process of that device and the evaluation of the fabricated device. This work was presented in [paper-I] and [paper-II]. The same simulation structure and fabricated component was used for the non-linear capacitance analysis in [paper-III], the large-signal TCAD methods developed in [paper-IV] to [paper-VI] and the bias-modulated measurement system described in [paper-VIII].

3.1 Device Outline

The main idea with the project was to design the LDMOS in a standard 0.35 µm Bi-CMOS process creating the p-well using an angular implant. An extended field oxide was used to create the drift region of the LDMOS transistor enabling higher field and hence higher drain-voltage. A cross-section is shown in figure 3.1.

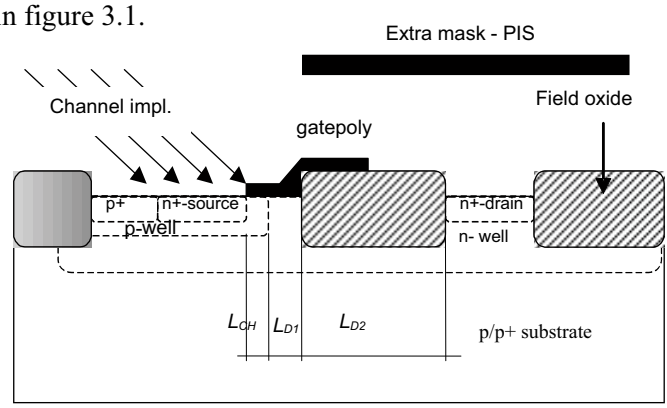

Figure 3.1. Cross-section of the LDMOS device structure with the suggested channel implant and extended drift region.

Structures with three different predicted channel lengths, $L_{CH,}$ of 0.2 µm, 0.3 µm and 0.4 µm were fabricated with three different drain drift-region lengths, L_{D2}, of 1.0 µm, 1.5 µm and 2.2 µm. In order to optimize the device for high frequency and high voltage operation the suggested structure was simulated using the commercial TCAD simulators Athena and Atlas from Silvaco [36], [37]. The device was then manufactured and evaluated with respect to design geometries and electrical performance. This information was fed back into the simulators for generation of a more accurate simulation structure for improved electrical and functional analysis. The input from the fabricated devices enabled a tuning of the different models used in the electrical simulator. This provided a more accurate simulation response for further analysis and improvement of the device design.

3.2 Device Evaluation

The devices were fabricated in the 0.35 µm BiCMOS process at Ericsson Microelectronics (that later became Infineon) [paper I]. The unique angular p-well implant was conducted as a split with implant dose and energy values spread around the values found from the process simulations. Results from the optimum dose and implant energy were presented in [paper-I] and [paper-II]. Measurements were conducted on-wafer using a manual probe-station mostly with a thermal chuck. They were conducted on a 10 finger test structure with a total gate-width of 0.4 mm. For the high-frequency small-signal measurements open de-embedding was used to reduce the effect of pad-parasitics [48], [49]. Some spread was found across the wafers but typical values are presented in the papers.

A large discrepancy was found between the TCAD simulated results and the measured results [paper-III]. Figure 3.2 shows the extracted input capacitance compared to the TCAD simulated input capacitance.

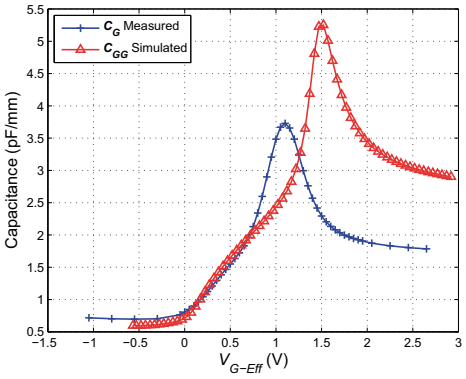

Figure 3.2. Input capacitance extracted from small-signal measurements compared to TCAD simulations for the angular implanted device at V_D= 12 V.

For high gate voltage the input capacitance consists of the pure oxide capacitance, $C_{OX,}$ [paper-III]. It can be calculated from the dielectric coefficient of the oxide, ε_{OX}, and its thickness, d_{OX} (3.12), [40].

$$C_{OX} = \frac{\varepsilon_{OX}}{d_{OX}} \qquad (3.12)$$

The oxide capacitance is approximately 1.5 pF/mm gate-width for the measured device and 2.7 pF/mm gate-width for the simulated structure. This discrepancy is caused partly by a difference in gate-overlap, L_{CH} and L_{D1} in figure 3.1 between the fabricated structure and the simulated one. It is also caused by a possible difference in gate oxide thickness between the fabricated and the simulated device.

3.3 Technology Summary with Results

The work done producing an angular implanted LDMOS transistor in a normal BiCMOS process have shown that it is a plausible solution. It has been possible to use TCAD for the initial design and optimization even though the process simulations did not produce an identical structure compared to the fabricated device. Device simulations did not provided absolute accuracy mainly due to the difficulty in modeling some of the process steps and the graded channel doping. This is a time issue. The models could have been improved for improved correlation. TCAD simulations have however provided sufficient results to make fabrication possible and for detailed qualitative analysis of the device. A summary of the power performance for this LDMOS technology from [paper-I] and [paper-VIII] is shown in table 3.1.

Class	L_{D2} (μm)	V_S (V)	f (GHz)	P_{OUT} (dBm)	G (dB)	η_D (%)	Ref.	Year
AB	1.0	12	1.9	20*	22	43	[Paper-I]	2002
AB	1.0	12	2.45	17*	21	28	[Paper-I]	2002
AB	1.0	12	3.0	15*	20	20	[Paper-I]	2002
AB	1.0	12	2.14	17*	19	27	[Paper-VIII]	2008
AB	1.0	12	2.14	10	21	12	[Paper-VIII]	2008
ET	1.0	PM	2.14	10	16	27	[Paper-VIII]	2008
AB	1.0	12	2.14	6	22	7	[Paper-VIII]	2008
ET	1.0	PM	2.14	6	15	20	[Paper-VIII]	2008

Table. 3.1. Summary of the power evaluations conducted for the LDMOS transistor. * are measured at 1 dB compression point. ET= Envelope tracking. PM = power model.

Compared to recent LDMOS devices the power and efficiency figures are low for this 2001 technology. Even so adding bias-modulation clearly shows the possibility for efficiency improvement. In the mid-power range the increase in drain-efficiency is as much as 15 % using bias-modulation [paper-VIII].

LDMOS transistors are also used for high or medium voltage switching applications like power supplies. In these applications an important parameter is the product of the breakdown voltage and the cut-off frequency, $BV*f_T$. The values for this LMDOS technology are presented in table 3.2.

Device	f_T (GHz)	BV (V)	f_T*BV (GHzV)
1.0 µm	13.38	41	548
1.5 µm	12.98	50	649
2.2 µm	12.36	63	779

Table. 3.2. Summary of breakdown-RF performance for the angular implanted device. f_T is measured at 12 V supply-voltage.

The devices produced in this work have shown a very high value for this product. Until 2006 the previously reported maximum value was 630 GHzV [50].

The possibility of integrating an LDMOS in a BiCMOS process was considered a viable solution for integrated power amplifiers at RF in 2001 when the work was initiated. The idea was to bring in the LDMOS module in the BiCMOS library and make fully integrated power amplifiers for medium power applications. Today this approach is abandoned for RF-circuits. Libraries of passives components have instead been implemented in the LDMOS processing to make integrated analog power amplifier solutions [51].

4. Load-Pull

Large-signal simulations or measurements are conducted to investigate how a device behaves under true operating conditions. For an RF-power transistor this includes analyzing parameters like, gain, noise and efficiency but also non-linearities. Working at radio frequency the wavelength of the signal is of the same dimension as the lines carrying the signal. This give rise to wave propagation along the lines and transmission line theory has to be considered [52]. The voltage and current along a line then depends on the position where and the time instance when it is measured. Controlled operating conditions for an RF transistor therefore includes besides biasing a certain source impedance, Z_S, and load impedance, Z_L, for the transistor to see in defined reference planes as shown in figure 4.1, [53].

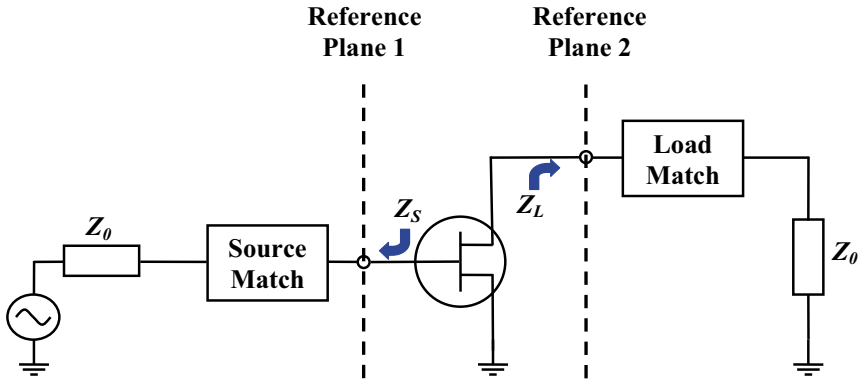

Figure 4.1. Schematic outline of a transistor in an amplifier configuration.

The reference planes usually constitute an easily accessible interface point. For a packaged device it would be the package leads. In a simulation the reference-planes are well defined as the gate and drain contacts of the FEM structure (if a common source configuration is used). In fabricated RF-power devices the reference planes are not so well defined due to the large area the leads cover. They are far from a point contact and may behave differently depending on the shape and size of the matching pad on the board they are mounted. This makes packaged RF-power device measurements tricky.

The behavior of a full amplifier depends on what impedances the transistor sees in the reference-planes. Building an amplifier means creating correct impedances to produce an amplifier with certain specifications like

noise, gain or efficiency. Normally it is done by making source and load impedance-transforming networks to create the wanted values from the characteristic impedance, Z_0, of the system in which the amplifier is going to be used (normally 50 Ω). For a small-signal transistor gain and noise are linear parameters. Amplifier response as a function of source and load impedance can be predicted from the small-signal s-parameters and noise data, simulated or measured. In large-signal operation there is no longer a linear response from the transistor. Power is generated at harmonic frequencies and the impedances the harmonics sees will also affect the overall response of the transistor. Gain, efficiency and non-linearities become functions of the source and load -impedances. The process of evaluating transistor parameters as a function of load and source -impedance is called load-pull (which generally also includes the source-pull).

Any impedance can be represented as a reflection-coefficient in that reference-plane related to the characteristic impedance (4.1) and (4.2), [52].

$$\Gamma_s(\omega)_{P1} = \frac{Z_S(\omega)_{P1} - Z_0}{Z_S(\omega)_{P1} + Z_0} \tag{4.1}$$

$$\Gamma_L(\omega)_{P2} = \frac{Z_L(\omega)_{P2} - Z_0}{Z_L(\omega)_{P2} + Z_0} \tag{4.2}$$

$Z_L(\omega)$ and $Z_S(\omega)$ are the respective impedances seen in the same direction in the reference-planes and are found from the voltage and current in that position, P, (4.3).

$$Z_P(\omega) = \frac{V_P(\omega)}{I_P(\omega)} \tag{4.3}$$

The reflection-coefficient is position and frequency dependant and relate to the incident, V^+, and reflected V^-, voltage-waves in that reference plane as shown in figure 4.2 and equation (4.4),[52].

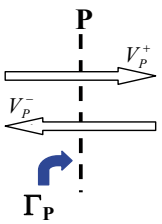

Figure 4.2. Reflection-coefficient in reference plane P.

$$\Gamma_P = \frac{V_P^-}{V_P^+} \tag{4.4}$$

If the reflection-coefficient is known the corresponding impedance can be found from (4.5).

$$Z_P(\omega) = Z_0 \frac{1+\Gamma_P(\omega)}{1-\Gamma_P(\omega)} \qquad (4.5)$$

In order to change the impedance seen in a reference-plane one therefore has to change either the voltage or current in that plane (from eq. 4.3) or change the incident or reflected voltage-wave (from eq. 4.4). One follows from the other. In simulations the voltage at a certain node can be forced to a specific value thereby changing the impedance. In measurements the reference-plane is usually not directly accessible and time-varying voltage and current measurements are tricky. In load-pull measurements the reflection-coefficients are therefore changed forcing the reference-plane node voltage and current to different values that indirectly change the impedance.

In a more general sense the behavior of the transistor in large-signal operation is a function of many parameters shown in figure 4.3.

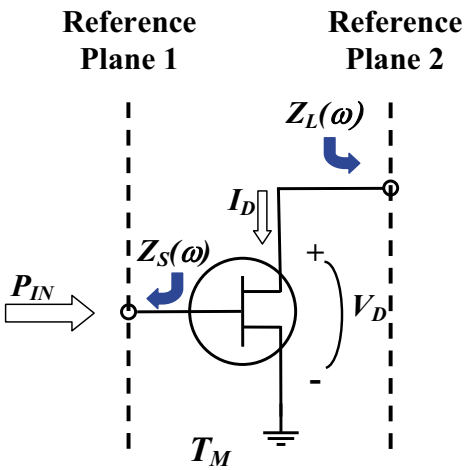

Figure 4.3. Parameters to monitor or control in large-signal RF-measurements and simulations.

These parameters include DC-bias (that specifies class of operation), input power, temperature, source and load impedances related to the reference plane. Some of these parameters are also time-dependant. This give rise to what is commonly known as memory-effects. A previous state of the transistor causes it to behave differently under similar stimuli and environment at two different occasions. Memory effects can be more or less

important to consider depending on the time-constant of the mechanism causing it and the bandwidth of the signal.

The impedances need to be specified for all frequencies where power is generated. Improper harmonic terminations cause harmonic reflections that combine with the wanted signal unfavorably and decrease performance. Proper termination of harmonics can on the other hand improve performance in some aspect. A properly terminated 3rd harmonic can for example increase the efficiency by creating a more square-wave voltage (class-F), [15], [18]. The source and load impedances therefore ideally need to be controllable at all frequencies (4.6) and (4.7).

$$Z_S(\omega) = \begin{matrix} Z_S(\omega_0) \\ Z_S(2\omega_0) \\ Z_S(3\omega_0) \\ \cdots\cdots\cdots \end{matrix} \tag{4.6}$$

$$Z_L(\omega) = \begin{matrix} Z_L(\omega_0) \\ Z_L(2\omega_0) \\ Z_L(3\omega_0) \\ \cdots\cdots\cdots \end{matrix} \tag{4.7}$$

Being able to control them is referred to as harmonic load and source pull. The lowest harmonics have the largest impact and are therefore most important to control, [15].

For multi-tone or wideband signals power is generated at mixing products out of band. These also need to be properly impedance-matched. These modulation or base-band impedances have shown to have a large impact on memory-effects in wideband systems [54], [55]. In a built amplifier these low frequency impedances (<60MHz) are usually filtered through the bias-network of the amplifier. A full control load-pull measurement system therefore needs wideband bias solutions with controllable impedance. In a simulation environment creating these impedances is more about finding a matching network capable of representing all impedances over the full band in a limited simulation setup. Most load-pull simulations are conducted in circuit simulators on extracted large-signal models. The models are generally extracted from multi-bias point, small-signal measurements and verified using load-pull. Computational load-pull is the only method to gain knowledge of RF-power performance pre-fabrication.

4.1 Computational Load-Pull

TCAD simulations have been tremendously successful in aiding in the design of new components since the mid 80s. Originally developed at universities as simple 1D simulators they have developed to full 3D commercial products with models for most materials and processing-steps and automatic mesh generation Being based on finite element methods they can be time consuming for good accuracy but with improved computer performance and computation algorithms even large-signal simulations for RF-power devices are now feasible on ordinary personal computers. There are two main methods of conducting large-signal TCAD simulations. Harmonic-balance, HB, and transient simulation based large-signal time-domain, LSTD.

4.1.1 Harmonic-Balance

Harmonic-balance is a non-linear simulation method that has been used in frequency domain circuit simulators for a number of years [56]. It is today the dominating non-linear method in commercial products like Agilent-EEsof ADS, Microwave Office and Ansoft Designer. TCAD simulators have traditionally been based on time-domain simulations. Due to the fast algorithms associated with HB attempts have been made to implement it in FEM based TCAD device simulators. Since HB involves solving for the Fourier -coefficients in the frequency domain the basic equations have had to be transformed from the time-domain, [57]- [63]. Much effort has been spent on improving the solution algorithms of the vast matrices created in the solution process. The main advantage of HB compared to LSTD is the computational speed for simulations of signals with vastly different frequency components like two-tone simulations at RF with narrow tone spacing. With HB a steady state solution can be found much faster than using LSTD since the simulation involves the same number of coefficients regardless of their frequency. HB provides an accurate steady state solution but it does not represent the actual time dependent voltage and current waveform during transient start up. It is today not included as a standard tool in any of the large commercial TCAD packages. Alone HB can not solve for signals with non-commensurate frequencies i.e. signals that are not harmonics of the same fundamental like digitally modulated signals, [56], but methods have been developed that adapts the HB method also for these applications [64].

4.1.2 Large-Signal Time Domain

Most commercial TCAD packages work according to the same principle. They solve Poissons equation and carrier continuity equations for a finite element model describing the physical device structure including material

properties and doping concentration. The simulations are solved in time-domain using the differential-form of the equations [37]. The circuit can be simulated for at a certain time-instant using transient simulation in the setup. Additional circuit components, passive or active, can be added to the simulation in a Spice like manner using mixed-mode simulation. In mixed-mode the TCAD element becomes just another simulation object in the netlist, numerically solved for every time-instance in the simulation. By building a matching circuit connected to the device the transient build-up and final steady-state time solution can be simulated producing the large-signal response [65]. The method is referred to as large-signal time-domain, LSTD. By changing the matching circuit connected to the device the time-domain response can be found for different loads and computational load pull, CLP, is conducted [66]. Fig. 4.4 shows a normal transistor measurements setup where DC is supplied though a bias-network separating the RF-signal from the DC feed using a bias-tee.

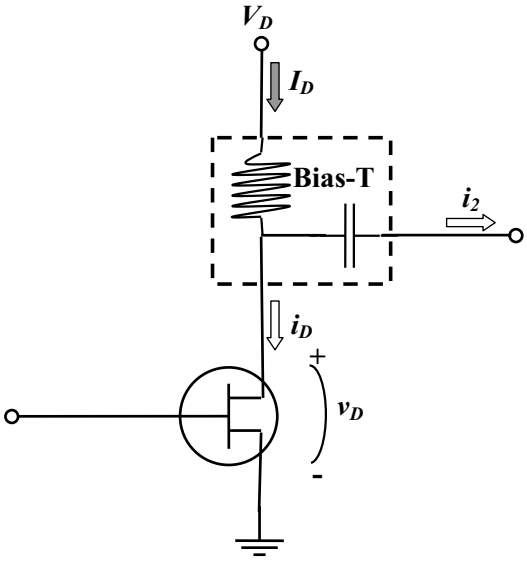

Figure 4.4 Normal measurement setup showing the bias-tee for separation of DC feed and RF signals on the transistor output.

In the LSTD computational load-pull setup the bias-tee is eliminated and DC is fed though the load to cut simulation time. This produces the currents and voltages shown in Figure 4.5.

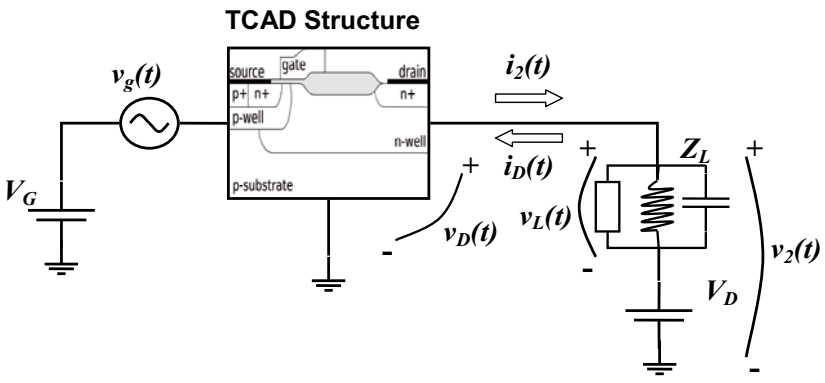

Figure 4.5. TCAD simulation setup with output currents and voltages.

Noticeable in this case are the simplified relationship that the output current $i_2(t)$ is merely the negative (same but in opposite direction) of the drain current $i_D(t)$, which is true only for the RF signals in the normal measurements due to the DC-block capacitor in the bias-tee (4.8),

$$i_2(t) + i_D(t) = 0 \tag{4.8}$$

The drain voltage $v_D(t)$ is equal to the voltage across the load $v_L(t)$ plus the drain supply voltage V_D, (4.9) and (4.10),

$$v_D(t) - v_2(t) = 0 \tag{4.9}$$

where

$$v_2(t) - v_L(t) - V_D = 0 \tag{4.10}$$

Since the inductor shortens the load for DC no voltage drop is present at DC across the load. Hence the circuit functions as a bias-tee except that the load itself provides the DC-feed.

4.1.3 General Algorithm for CLP

In transient simulations for RF-power a steady-state response over the load first needs to be established. Depending on the nature of the load this can take several periods. An example for an active load is shown in figure 4.6.

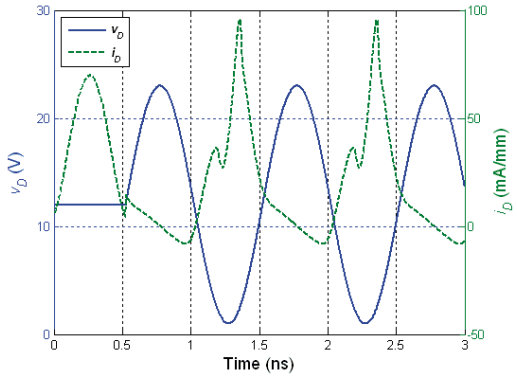

Figure 4.6. Startup to steady-state for an active load close to the 1 dB compression point.

The first half period was here used to establish the phase relationship between the gate-voltage and the time-varying drain-voltage. During transient simulations in TCAD the time-step between two consecutive solutions is reduced until a steady-state solution can be found for a time-instant. As a result the time-series include unequal time-steps unfavorable for FFT. The time series are therefore re-sampled with equidistant samples using the cubic spline interpolation (piecewise polynomial form) [67]. This is part of the post-processing and conducted in a mathematical tool like Matlab or Octave. An example of re-sampling is shown in figure 4.7.

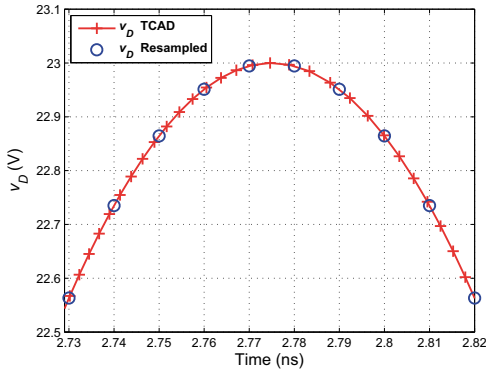

Figure 4.7. Drain voltage from LSTD simulations and re-sampled using cubic spline interpolation.

Due to the period nature of the signal period sampling is used with oversampling to cover all interesting harmonics. The FFT is conducted at exactly one period rendering no need of windowing functions [68]. This produces a discrete (line) spectrum of the voltages and currents.

From the frequency components of the input and output voltage and current the output power, P_{OUT}, drain efficiency, η_D, phase difference, $\Delta\Phi$, and impedance, Z_L, can be calculated, (4.11)-(4.14),

$$P_{OUT}(\omega) = \frac{1}{2}\mathrm{Re}\left(\left[V_2(\omega)\right]\left[I_2(\omega)\right]^*\right) \qquad (4.11)$$

$$\eta_D = \frac{P_{OUT}(\omega_0)}{P_{DC}} = \frac{P_{OUT}(\omega_0)}{V_{DC}I_{DC}} \qquad (4.12)$$

.

$$Z_L(\omega) = \frac{V_2(\omega)}{I_2(\omega)} \qquad (4.13)$$

$$\Delta\phi = phase\left(I_2(\omega_0)\right) - phase\left(V_1(\omega_0)\right) \qquad (4.14)$$

From multiple simulations with different load-impedances load-pull contours can be created showing any parameter as a function of impedance. Much information is also revealed from time-domain series themselves. The power dissipated in the device can be expressed as a function of the time-domain waveforms over the device (4.15), [56]

$$P_D = \frac{1}{T}\int_0^T v_D(t)i_D(t)dt \qquad (4.15)$$

P_D is the dissipated power and T is the period-time of the waveform. The RF power delivered to the load can be computed from the time-domain waveforms of the output current and voltage (4.16).

$$P_{RF} = \frac{1}{T}\int_0^T \left(v_2(t) - V_D\right)\left(i_D(t) - I_D\right)dt \qquad (4.16)$$

Note that from the time-domain series the full RF power delivered to the load is computed including the power of all harmonics. The post-processing includes dealing with time-domain to frequency-domain conversions. It is necessary to always maintain the energy-balance stipulated by Parseval's theorem (4.17), [69].

$$\sum_{n=-\infty}^{\infty} \left|x(n)\right|^2 = \frac{1}{2\pi}\int_{-\pi}^{\pi} \left|X\left(e^{j\omega}\right)\right|^2 d\omega \qquad (4.17)$$

It states that the sum of the square of the time-domain samples, *x(n)*, are equal to the integral of the square of their Fourier-transform, $X(e^{j\omega})$.

With transient simulations the device can basically be excited by any time varying signal, sinusoidal, two-tone or any more complex modulation. For non-periodic signals window functions have to be implemented before the FFT to minimized energy in the finites length time series [68], [69]. It is feasible with device simulation of non-linear behavior like intermodulation distortion. Since a full period is needed for the FFT the number of points necessary to simulate becomes excessive and impractical for RF two-tone simulations with narrow tone-spacing. For digitally modulated signals the number of symbols needed to simulate for good accuracy is great and these simulations are still impractical but with improving computational power of more modern computers it will be feasible in a near future.

4.1.4 Computational Source-Pull

Since the power is generated on the output the source side is generally not considered for RF-power, LS-TD simulations. Instead the output response is related to a swept or constant voltage on the device input. This simplification reduces the simulation time drastically. From a power perspective this model assumes constant input impedance. Full circuit with input matching network shown in figure 4.8 can be used but the complexity of the circuit and the limitations in Q-value makes the simulations very time consuming.

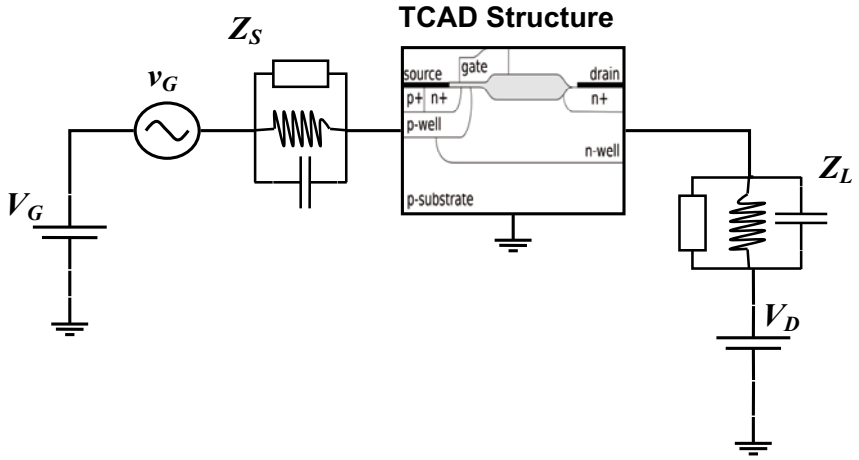

Figure 4.8. Full circuit mixed-mode simulation source and load impedance match.

For most investigations a study of the output circuit is sufficient and the simplified source model with directly applied voltage is no limitation.

4.1.5 Load-Pull Setups

There are many ways to configure the mixed-mode simulation for computational load-pull. Usually a combination has to be used to get most information from the simulation in limited amount of time.

Computation Passive Load-Pull

The first TCAD mixed-mode LSTD simulations for RF-power transistors included a resonance circuit producing the desired load impedance at the actual frequency of interest as shown in figure 4.9, [65].

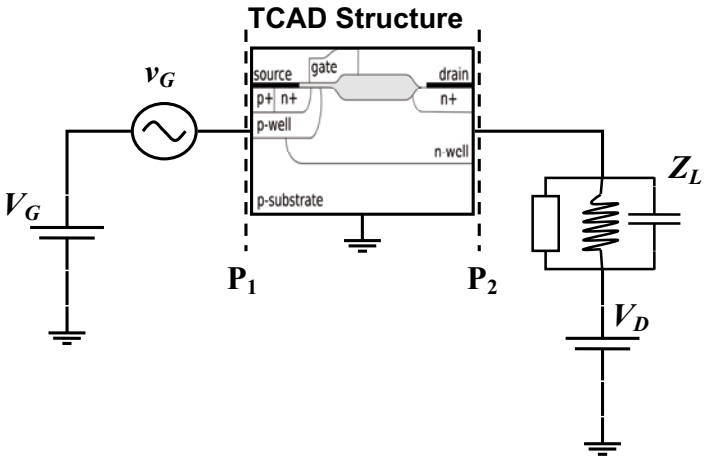

Figure 4.9. Simulation setup for passive computational load-pull for fundamental load.

The voltage in the reference node (plane P_2) is built up from startup by the charging of the resonator. At steady-state the impedance is formed from the phase and magnitude relationship between the voltage over the load and current entering the load from (4.3). Typical startup is shown in figure 4.10.

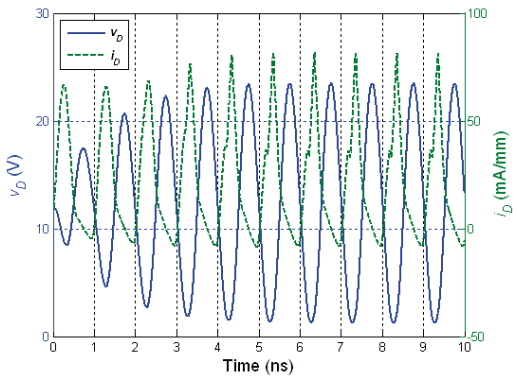

Figure 4.10. Startup to steady-state for passive load Q=5 close to the 1 dB compression point.

The Q-value of the resonance circuit is inversely proportional to the settling time for steady-state which favors the use of low-Q resonators. A low Q-value will however decrease isolation and hence possibly affect the harmonic impedances. A typical example is shown in figure 4.11.

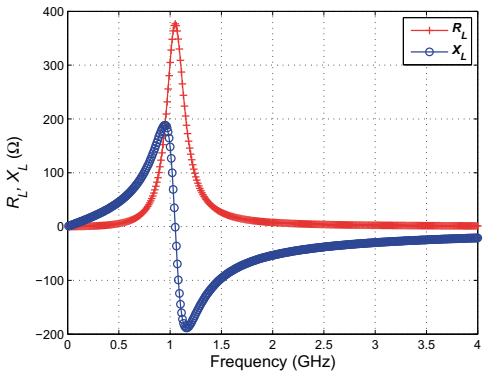

Figure 4.11. Impedance for a Q=5 parallel resonator with $Z_L(\omega_0)$=(305+ j148) Ω.

The Q-value of the resonance circuit relates to the resonance frequency of the resonator which is different than the fundamental simulation frequency since the load is not purely resistive. The main advantage using a passive load is that the response from a transient LSTD simulation represents the actual voltage and current waveforms for the circuit also during start-up conditions and that the load-impedance is linear i.e. it does not change with input power. In that it much resembles the function of a passive load-tuner in a traditional load-pull system. The obvious drawback of passive loads is the lengthy simulation time. Even for moderate Q-values several periods have to be simulated before steady-state is reached and every impedance point may take several hours to simulate on modern workstations depending on the complexity of the device and the accuracy needed.

The lengthy simulations make parallel resonators less suitable for actual load-pull when the optimum impedance is to be found. For power sweeps they are ideal since they create the same impedance regardless of power-level.

Computational Active Load-Pull

During large-signal operation the current generated in the device produces a voltage swing over the load on the output. Instead of connecting a load on the output it is possible to directly connect a time-varying voltage generator at the same frequency as the stimuli signal on the gate as shown in figure 4.12. This setup was suggested in [66] as computational load-pull and later developed further in [70].

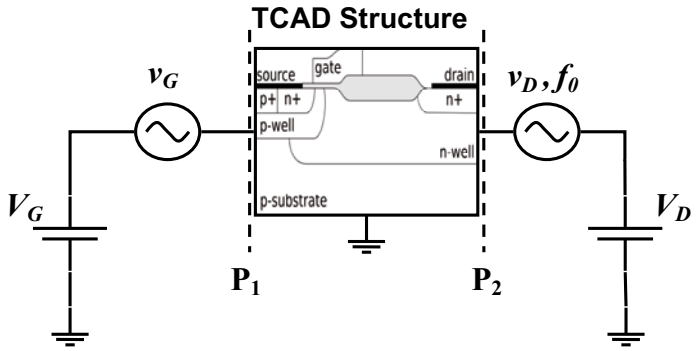

Figure 4.12. Simulation setup for active computational load-pull for fundamental load.

By changing the delay and amplitude of the applied voltage v_D the phase and magnitude is changed between this voltage and the output current i_2 and hence the impedance seen by the component changes (4.3). The voltage swing is applied to the output and does not have to be built up by a resonance circuit. Therefore the simulation reaches steady-state much faster than for a passive load. Since the output voltage only contains components at the fundamental frequency this setup implies that all harmonics are shorted. Hence it produces a nice sinusoidal output voltage signal. Three simulations periods is usually sufficient where the last can be used for FFT analysis. This method much resembles the use of an active load in Load-Pull measurements based on the split signal method, [71]. It suffers from the same drawback, i.e. the inability to in advance predict what impedance is created from a certain combination of stimuli signals. This can be overcome by tuning the output voltage amplitude for a certain impedance response during simulation but this increases simulation time. More efficient is to use the method in the same manner as when doing load-pull measurements i.e. making measurements at a number of points and then post-process to identify impedance and extract optimum point. This finds the optimum point at a fixed input voltage (power in the load-pull measurement case). For swept input voltage it is however more tricky. Either the output voltage, v_D, is tuned during simulation to desired impedance or the impedances are found using post-processing with extraction of a the full sweep from a number of constant input voltage measurements.

The fast simulations and the consistent termination of harmonics make active loads very suitable for load-pull when the optimum impedance is to be found. For power sweeps they are less useful due to the changing impedance with input power. This method was used both for the LDMOS analysis [paper-III] and the LDMOS on SOI analysis [paper-VII]. A typical example of load-pull contours generated from active computational load-pull is shown in figure 4.13.

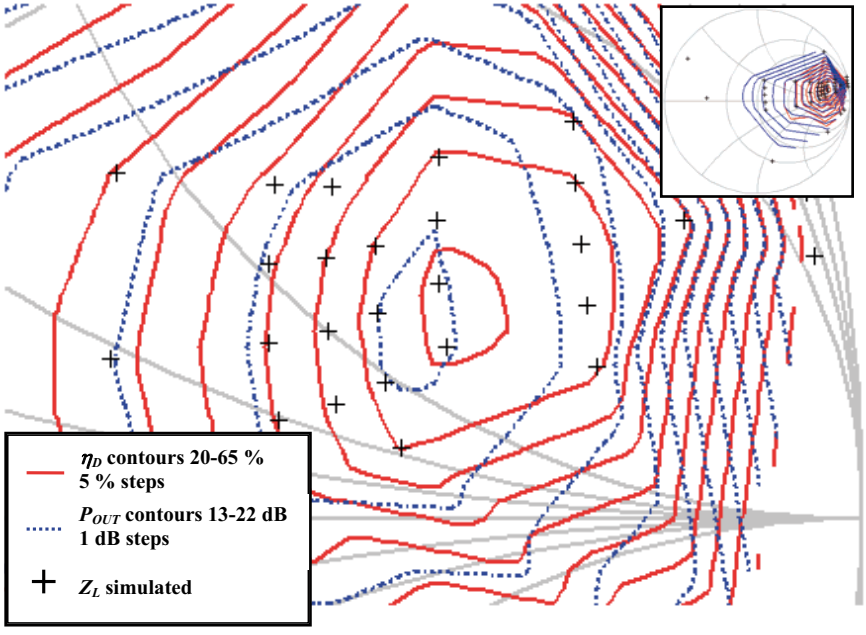

Figure 4.13. Computational load-pull contours for the angular implanted LDMOS in class AB, V_D =12 V, at 1 GHz. Sub-plot show position in impedance Smith-chart.

Computational Two-tone Simulations

Two-tone simulations are made to study intermodulation distortion. Once the optimum load-impedance is found from computation load-pull a two-tone simulation can be conducted with the optimum load impedance created from a parallel resonance circuit using the setup shown in figure 4.14.

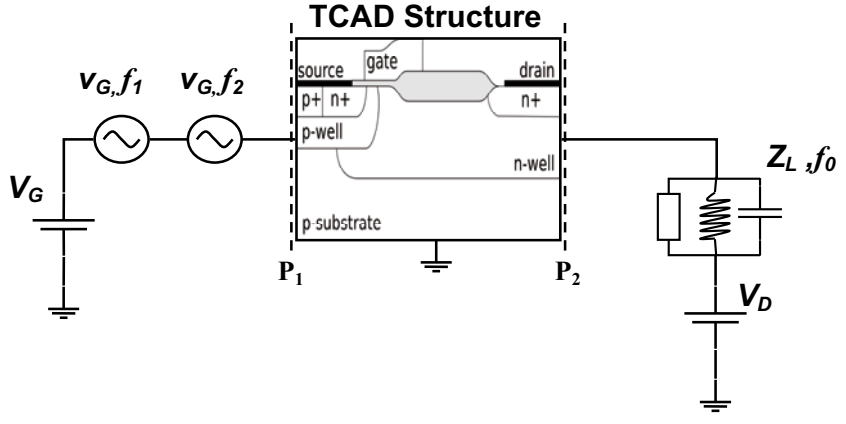

Figure 4.14. Simulation setup for two-tone simulations with passive load.

LSTD simulations need to be conducted for one full modulation cycle in order to make the FFT properly. For a two-tone simulation with narrow tone spacing the simulations therefore are lengthy in time. If the tone spacing in increased there is a risk that the two-tones are amplified differently due to the limited gain-flatness of the device. The bandwidth of the load is also important. With large tone-spacing the impedance seen at the two frequencies will differ. The power of the intermodulation products can be calculated from the Fourier coefficients at the intermodulation samples (4.18)-(4.21).

$$IM3_{Low} = \frac{1}{2}\mathrm{Re}\left(\left[V_2(2\omega_1 - \omega_2)\right]\left[I_2(2\omega_1 - \omega_2)\right]^*\right) \quad (4.18)$$

$$IM3_{High} = \frac{1}{2}\mathrm{Re}\left(\left[V_2(2\omega_2 - \omega_1)\right]\left[I_2(2\omega_2 - \omega_1)\right]^*\right) \quad (4.19)$$

$$IM5_{Low} = \frac{1}{2}\mathrm{Re}\left(\left[V_2(3\omega_1 - 2\omega_2)\right]\left[I_2(3\omega_1 - 2\omega_2)\right]^*\right) \quad (4.20)$$

$$IM5_{High} = \frac{1}{2}\mathrm{Re}\left(\left[V_2(3\omega_2 - 2\omega_1)\right]\left[I_2(3\omega_2 - 2\omega_1)\right]^*\right) \quad (4.21)$$

This is possible also for higher intermodulation products. Note that it is possible to separate the low intermodulation products from the high. Possible sideband asymmetries are therefore identifiably. The parallel resonance circuit will also create load-impedance for the power generated at the mixing frequencies and modulation band frequency. This makes the two-tone setup ideal for investigations of possible intrinsic device memory-effects. Two-tone simulations were conducted in [paper III] and as reference in [paper V].

Computational Harmonic Load-Pull

In some cases it is important to be able to control the harmonic impedances. In class-F applications proper harmonic load impedances are used to increase the efficiency, [15], [72]. For the harmonic investigation it is important to separately be able to control the harmonics therefore good isolation is needed between the loads. This can be compared to actual harmonic load-pull measurements where good isolation is needed in the triplex-filter separating the fundamental load impedance from the harmonic impedances, [73], [74]. Using an active load the load impedance is a function of the controlled output voltage and the current produced by the stimuli signals (4.3). If a harmonic load has a direct impact on fundamental current it will hence affect the fundamental load impedance created. A passive load on the other hand is constant and remains the same regardless of stimuli signals if the isolation is good (high Q-value). A passive load is therefore used as

fundamental load during harmonic load-pull. Active loads are used as harmonic loads in order to decrease computational time. The computational harmonic load-pull is configured as shown in figure 4.15, [paper-VI].

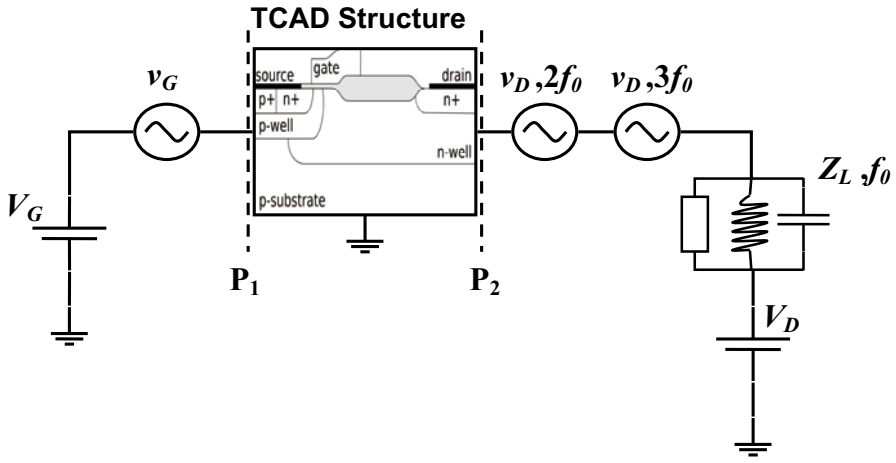

Figure 4.15. Simulation setup for computational harmonic load-pull with passive fundamental load and active harmonic loads.

A 3rd harmonic load-pull simulation of the angular implanted LDMOS device is shown in figure 4.16.

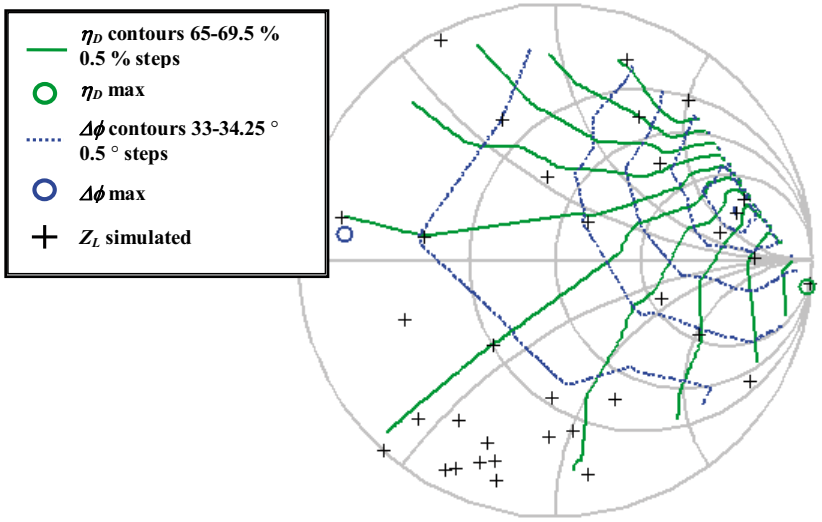

Figure 4.16. Computational 3nd harmonic load-pull contours for the angular implanted LDMOS in class AB, V_D =12 V, at 3 GHz. Simulations close to compression.

The values of the passive load at f_0 have to be carefully selected. A high Q-value with a long time constant takes longer time to reach steady-state. A low Q-value becomes more wideband and may have great impact on harmonic load impedances as shown in figure 4.12. If finite impedance exists from the f_0 resonant circuit at the harmonics the harmonic voltage sources for active load-pull will merely add to the already present harmonic voltage from the resonator. The harmonic impedance then becomes hard to predict. It is hence a trade-off between Q-value (simulation time) and predictability (time to result). This method was explored on the LDMOS device in [paper-VI].

Pulse and Switch-Mode LSTD Simulations

Recently class-C, pulse-mode simulations using LSTD have been presented [75]. In the setup a voltage-pulse was injected on the input. The setup used is shown in figure 4.17.

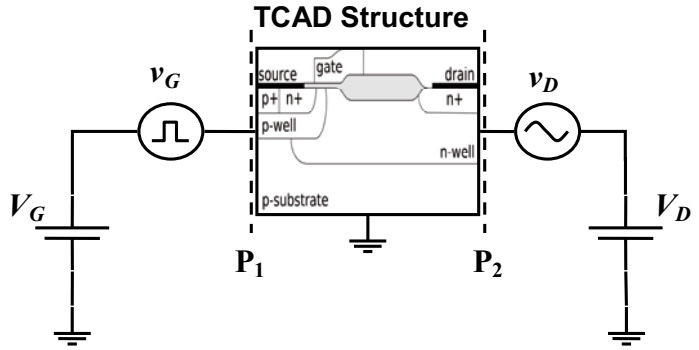

Figure 4.17. Simulation setup for pulse-mode RF-power LSTD simulations.

By directly creating a square-wave on the input the pulse-mode is recreated and the function of the device can be studied under pulse-mode conditions. A similar approach can be used for full switch-mode simulations. A pulse entered on the output would also generate the harmonic loads. For a 50 % duty cycle the pulse represents shorted even harmonics and open odd harmonics on the terminal. With this approach there is no way of separating the control of the harmonic loads.

LSTD Simulations with Bias-Modulation

For high-efficiency operation using architectures like envelope-tracking the device is working under varying bias-conditions. For a drain bias-modulated device the voltage dependency of the output capacitance place a big role in the performance. With a large drain bias dependency of the capacitance the optimum load matching varies and the gain will vary. This can be investigated using LSTD simulations with bias-modulation. How the drain bias should be modulated by the envelope needs to be modeled and that

modulated signal must be presented to the drain of the device. The most simple varying envelope signal is the sinusoidal amplitude modulation created by a two-tone. A simulation with drain bias-modulation can be conducted by synchronizing a voltage source on the output to the envelope of the two-tones on the input as shown in figure 4.18.

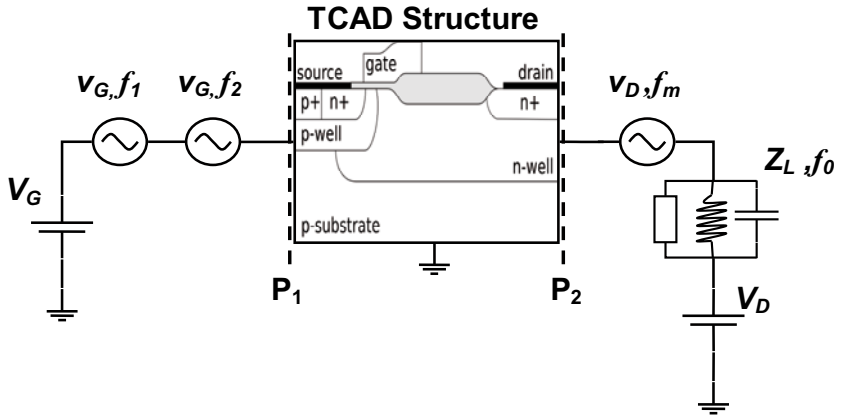

Figure 4.18. Setup for LSTD simulation of drain-bias modulation with passive load.

The parameters for the source creating the bias-modulation are set by the model of the modulator and pre-computed externally. A typical simulation input voltage close to compression is shown in figure 4.19.

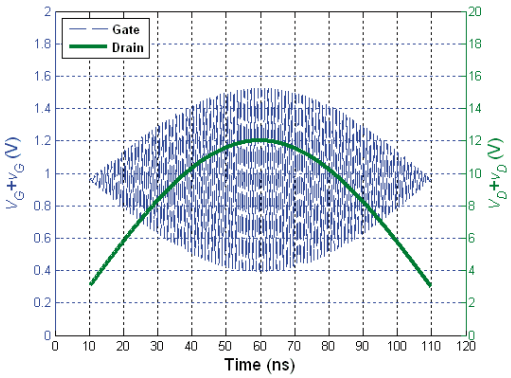

Figure 4.19. Gate voltage and modulated drain bias for TCAD, LSTD simulation with drain bias-modulation.

The possibility of this method was explored on the angular implanted LDMOS device in [paper-V]. Envelope-tracking is a complex system that not only affects the efficiency but also the linearity of the PA-system. One of the main advantages of studying bias-modulation in TCAD is that the transistor can be studied apart from any contribution by the modulating device.

Non-linear effects of delay in the bias can be studied by phase-shifting the bias-modulated signal.

4.1.6 Time and Accuracy

As always there is a tradeoff between simulation time and accuracy. In LSTD computational load-pull there are contributions to inaccuracy both from the TCAD simulation and from the algorithm in the post-processing.

TCAD Considerations

When the simulation in the TCAD environment is set-up a number of parameters have to be specified. Some relate to the actual device models and depend upon good calibration to measurement-data for improvement. Typical parameter that needs calibration is for example the recombination models and mobility models for the device. These model calibrations are best done based on DC-data. At some instance the models are considered good enough to represent the actual device. It may not be totally accurate but good enough to represent the mechanisms aimed to study.

Another set of parameters relate to the algorithm used in the simulation. A computation method has to be specified together with constraints for it. In mixed-mode simulations used in LSTD different variants of Newton algorithms are used for the solution [37]. If a solution does not converge for a certain time-instance the time-step is reduced and a solutions in sought closer to the previous solution. This is what cause the unequal time-steps in the TCAD solution. Even if a solution is found it may not provide an accurate answer. Numerous calculations are conducted for every point and there is a limit to how small values the simulator choose to consider in the solution and what is regarded as 0 and truncated. In Silvaco (Atlas) this can be specified in the setup as the maximum local truncation error, LTE. The LTE value has a large impact on the simulation time as shown in figure 4.20.

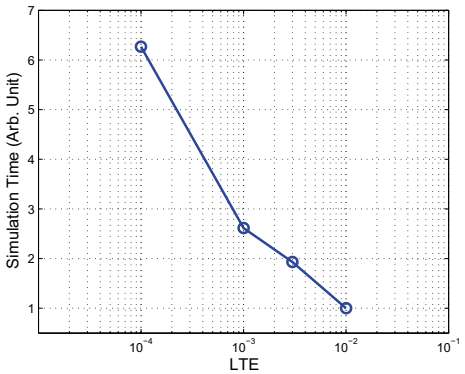

Figure 4.20. Relative simulation time for decreased local truncation error during LSTD simulation of a low amplitude (50 mV per tone) two-tone signal.

For large signals a large value can be used but for small signals it needs to be reduced to provide sufficient accuracy in for example intermodulation simulations. Therefore small signals creating fewer simulation points in the transient LSTD simulation still can take long time to simulate. The LTE value basically sets the limit for the dynamic range in the simulation. The number of points to simulate grows almost linearly with signal amplitude as seen in figure 4.21.

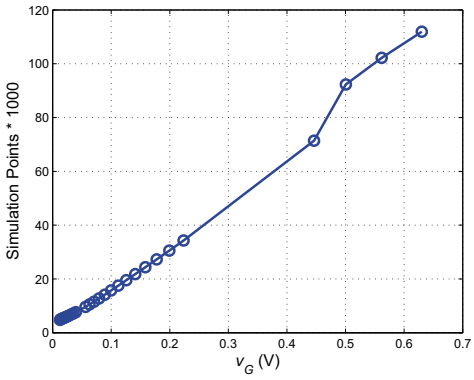

Figure 4.21. Number of simulation points versus individual tone amplitude for a 100 period two-tone simulation (10MHz spacing at 1 GHz).

The actual simulation time depends on TCAD structure, hardware, operating system and LTE value. A crude estimate is summarized in table 4.1 based on simulation of the angular implanted LDMOS with a FEM structure of about 7800 points (about 13500 triangles).

Processor	**Speed (GHz)**	**Number of Processors**	**Time per Point (s)**
P4	2.4	1	17-20
Xeon (Quad)	3.0	1 (1 of 4)	13-16
Core2Duo	2.4	1 (1 of 2)	7-9

Table 4.1 Summary of time per point for different processor generations.

A typical active load simulation with low amplitude (v_G=0.1 V) would take about 1 hour to simulate on a Core2Duo. A high amplitude signal would take about 20 hours. Two-tone simulations with high amplitude and narrow spacing can take days or even weeks to simulate. With improved computer performance these figures are expected to drop drastically in a near future making more advanced simulations possible in reasonable time.

Post-Processing Considerations

In the post processing there are errors involved with the re-sampling of the signal and the surface interpolation in the impedance extraction process. Spline-interpolation has been used in the re-sampling process. The possible errors from this process are not fully analyzed yet. They are expected to cause problems mainly at higher harmonics. A more severe error is expected from the interpolation in the impedance-plane when the optimum impedance is located. If assumptions are made from a limited number of simulated impedance points or if bad contour algorithms are used the result may be too far from the optimum solution. Since that value is carried on to further simulations it may cause a large discrepancy in the end. To eliminate the possibility more impedance points should be simulated in the initial load-pull simulation. This can be done using an adaptable approach narrowing in on the peak. This approach was used for the fundamental frequency load-pull in [paper-VI].

4.1.7 Future Work

There are two main issues to address with LSTD computational load-pull for the future. At the moment CLP is only realistic for 2D structures. For 3D structures it is still too computationally heavy. The 2D interface provides access to the intrinsic device interior to any 3D or package parasitics. This is good since it makes it possible to identify fundamental mechanisms that are not as easily measured. For verification the simulations need to be compared to measurement data. A common interface needs to be established. Measurements are possible on small structures on wafer. A common interface would then be a small 3D structure with possible probe connections. That would enable direct verification with wafer measured load-pull data. Next step would be to also incorporate a package and make full transistor simulations. This would be a greater problem since the package with bond-wires would have to be modeled in a separate 3D field simulator.

The second issue concerns the simulation of digitally modulated signals. CLP has the capability to also include effects of wide-band signals. A suggested setup for analysis in the digital domain is shown in figure 4.22.

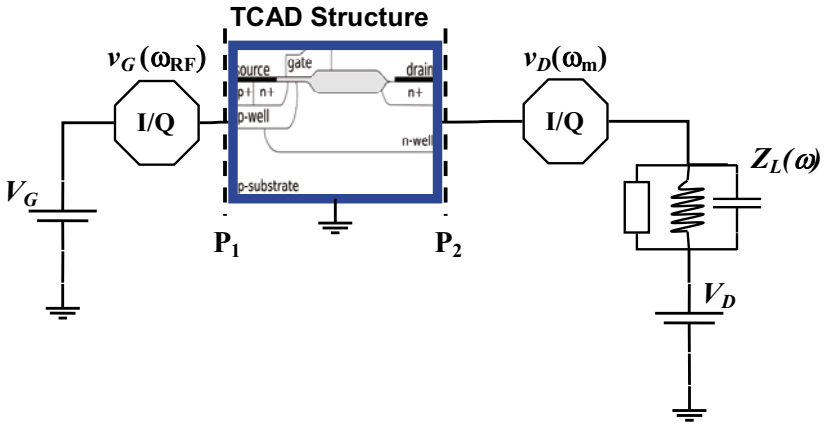

Figure 4.22. Suggested setup for LSTD simulation of digitally modulated signals with drain-bias modulation. Added 3D or package model indicted as blue rectangle.

The passive load will be generated to represent the wanted impedance at all frequencies. RF-samples for any digitally modulated signal are used as stimuli-signal entered through a time-data series. A possible drain bias-modulator is based on the envelope data from the RF-series on the gate. The FFT-algorithm needs to be modified to also handle non-periodical stochastic signals. With this system it would be possible to make detailed studies of non-linearities of digitally modulated signals like ACLR and sideband asymmetry. Today it is computationally too lengthy for good accuracy but with increased performance of the hardware it will be possible. Already today the TCAD software includes the possibility to generate arbitrary signals in transient simulations.

4.2 Load-Pull Measurements

Computational load-pull is an excellent tool to identify mechanism and explore the possibility of a technology. It is especially useful for relative comparison of devices. To fully evaluate the performance of fabricated devices and to verify the expected performance found in simulations, large-signal measurements under true operating conditions are necessary. In figure 4.3 the parameters that affect large-signal performance for RF-power devices where identified. All those parameters need to be monitored and the impedances need to be controlled. Today many methods and measurement systems coexist to provide the necessary information under large-signal conditions [76]. There are two main functions in all system, controlling the impedances at all bands of interest and monitoring the power at all relevant frequencies.

4.2.1 Separating the Impedances

Impedance tuning at all frequencies of interest is important. RF-impedances are traditionally separated using harmonic filters where the fundamental component is separated from the harmonics as shown in figure 4.23.

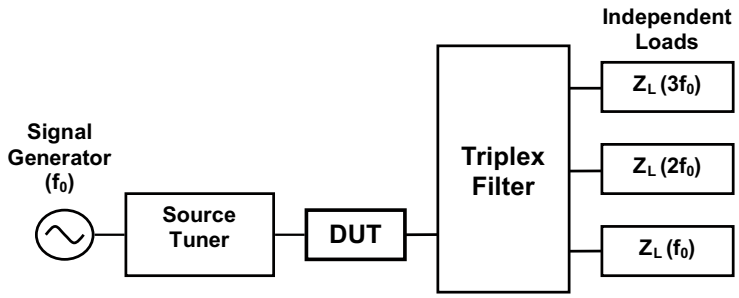

Figure 4.23. Harmonic load-pull setup with triplex-filter.

Then individual loads are presented for the different bands. Low insertion loss and high isolation are important parameter to make individual tuning possible and to maintain the high matching range created by the impedance tuning element [74], [77]. Some impedance tuning methods allow alternative ways to discriminated frequencies that are not based on normal filter technology.

Impedance tuning at envelope frequencies has become increasingly important with the discovery that these intermediate frequency, IF, (<60 MHz) impedances affect the non-linearities generated due to memory effects, [54], [55]. In a traditional load-pull system these frequencies have not been under control. DC has been supplied through bias-tees providing a low frequency path for the power supply as shown in figure 4.24.

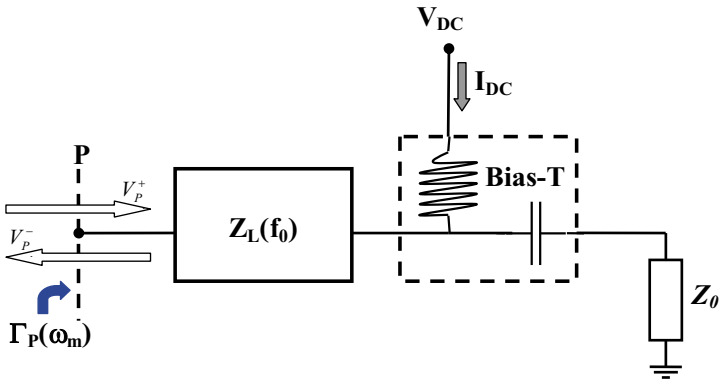

Figure 4.24. Harmonic triplex-filter response for a 2.15 GHz fundamental frequency filter.

The low-pass bias-tee provides a low-impedance path to the power supply for DC and low frequency. Depending on the cut-off frequency of the bias-tee it may cover the envelope frequency and represent part of the modulation-band impedance as shown in figure 4.25.

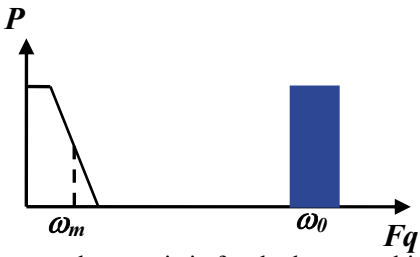

Figure 4.25. Frequency characteristic for the low-pass bias network

The optimum is to cover the full IF bandwidth in the low-frequency path and be able to control it. Original work in this field used IF and RF signal-separation in combination with active load-pull and time-domain IF impedance measurement using an oscilloscope [78]. More recent work includes dedicated advanced boards for signal separation including switch-banks of resistors for passive IF impedance control in combination with active load-pull [79]. In systems for bias-modulation it is absolutely necessary that the bias-tee provide a low impedance path for the full frequency band of the bias-modulation [paper-VIII].

4.2.2 Impedance Tuning

Controlling the impedances can be done in many ways. The first automated systems that were used for load-pull where based on stepper-engine controlled mechanical tuners. They are still mainstream today for high-

power. For medium power active load-pull systems are now used more widely. With improved hardware active load-pull is now even possible using multiple RF-generators with direct IQ control. This is also the basic principle of many of the network analyzers with multi-port or large signal capabilities that recently have come on the marked. Most important parameters for impedance tuning elements are matching-range, power-capability, repeatability and bandwidth.

Mechanical Tuners

A typical mechanical tuner is shown in figure 4.26.

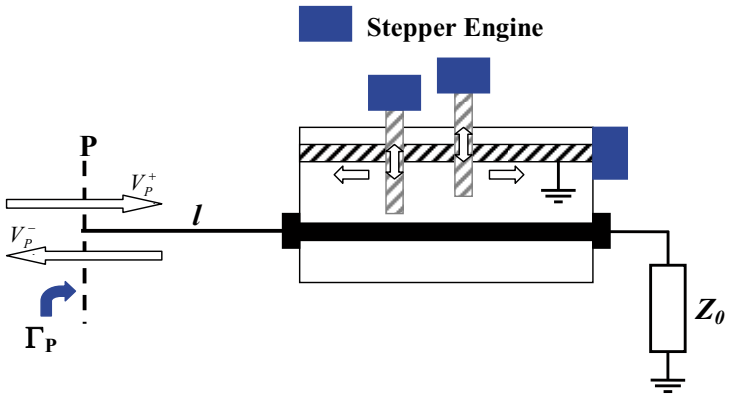

Figure 4.26. Principles of passive stepper engine controlled tuner.

By changing the depth of short circuiting slugs and their position along a transmission line basically any impedance can be created seen as any point in the Smith-chart in the reference-plane, P. The tuners and calibration is computer controlled with excellent repeatability. Calibration is done by measuring numerous impedance points using a vector network analyzer in-situ, or with the system broken apart. Connector repeatability is then very important and high- precision APC-7 connectors are usually used. Due to losses in the tuner reflections-coefficients are usually limited to $\Gamma<0.9$ (a voltage standing wave ratio, VSWR, about 20) but bandwidth limited systems optimized for certain bands can reach $\Gamma>0.95$ (VSWR >40). Today pre-matched systems exist with VSWR>100 able to match even to lowest impedance from high-power devices [80]. In the system some matching-range is lost in the cables or fixture between the tuner and the measurement reference-plane. For very high power devices with extremely low impedances (<1Ω) this can make proper matching impossible even with high matching-range tuners and impedance-transformers need to be used. Mechanical tuners exist with built-in harmonic-tuning capabilities based on sliding resonator technology [81]. The main advantages with passive tuners are their power-handling capabilities (>100W CW) and broadband nature.

Their main drawback is the slow process changing impedance point during measurement and calibration. They have excellent repeatability (>50 dB). Mechanical tuners are only used for the RF-tuning of source and load impedance.

Active Loads

Active loads exist in two main configurations with vastly different characteristic, open-loop systems and closed-loop systems. Their main advantage is the high speed with which the load can be changed and the possibility to reach Γ>1 and hence compensate for losses in the system making full matching possible at the DUT interface. Their common main drawback is the need for high power amplifiers. An open loop system is shown in figure 4.27.

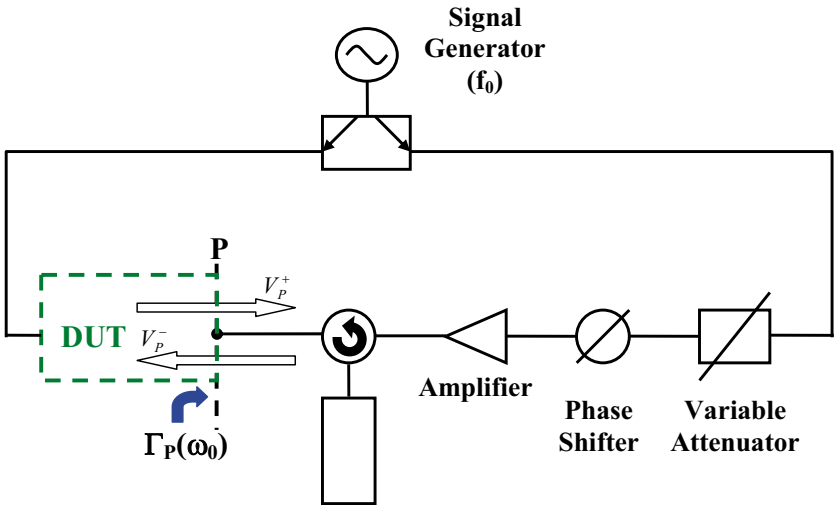

Figure 4.27. Outline of open-loop active load-pull system.

In the open-loop active load-pull system the stimuli-signal is split in two branches and part of it injected on the output of the device under test, DUT, [71]. By changing the phase and magnitude of the injected signal the impedance seen from the DUT is changed (4.4). Since the impedance is a function of the output signal generated from the DUT and injected signal it is impossible to know in advance what impedance an attenuator and phase setting will create. Therefore open-loop systems need to have an in-situ impedance monitoring system. Harmonic system uses frequency multipliers to generate the injected harmonic signals, [82],[83]. A more modern approach is to make the phase and amplitude change using an IQ-modulator or even injecting the signal directly from a signal generator with build in IQ-modulation.

For the closed loop system the injected signal on the output is a function of the output signal of the DUT through the gain and the phase shift of the closed loop as shown in figure 4.28, [84].

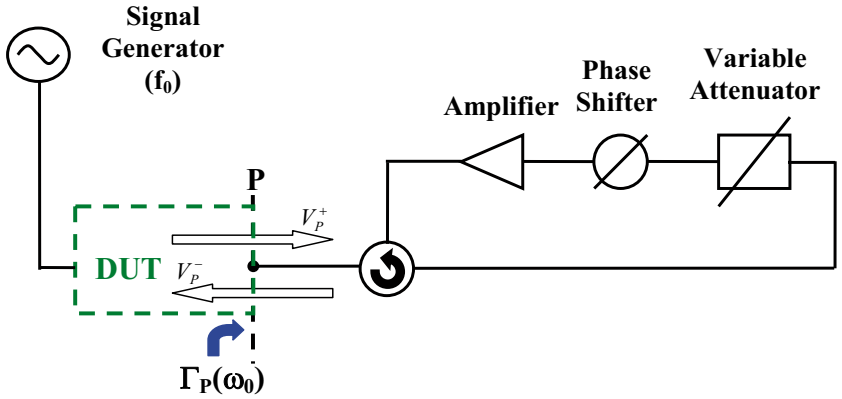

Figure 4.28. Outline of closed-loop active load-pull system.

The loop settings control the impedance seen. Due to the loop feedback closed-loop systems are inherently unstable but modern systems based on IQ modulators have addressed some of these problems, [85]. Loop delay is an important factor for large bandwidth measurements of modulates signals [79].

Active systems can be used both for RF impedance tuning and for IF tuning at envelope frequencies [79],[85]. Their power handling capability is limited mainly by the amplifier but is normally in the range of a few watts. Repeatability and linearity can be questioned but is not a major problem since active loads are used with in-situ impedance measurements (not pre-calibrated).

Solid-State Loads

An alternative way of producing impedance states is a controllable matrix of solid-state RF switches (PIN diodes) that combine and create different impedances. These loads are extremely fast and can provide excellent repeatability (-95dB). Their power handling capability is in the range of 10-30 W, [80]. The non-linear impedances created in combination with redundancy in the large number of impedance states (about 500 000) can be used for harmonic impedance tuning, [86]. Their main drawback is the non-linear impedances. They are mainly used in noise-characterization systems.

4.2.3 Power Monitoring

Somehow the power of the incident, reflected and transmitted signals need to be measured. This has traditionally been done using scalar measurements with RF power-meters through directional couplers or six-ports [87]. Today there are many options including instrumentation for direct waveform measurement of modulated signals.

Power Meters

Power meters provide is most simple measurement solution to monitor the power levels in the system. Modern sensors provide 90 dB dynamic-range for CW signals. For modulated signals sensor modulation bandwidth is normally about 5-30 MHz with a dynamic range of 50 dB to 18 GHz [88]. For lower frequencies (<6 GHz) high performance systems with 65 MHz bandwidth and 70 dB dynamic range exists, [89]. The main drawback using power-meters is the limited dynamic-range, measurement time and the inability to discriminate and measure power at different frequencies.

Spectrum Analyzers

In load-pull Spectrum analyzers have mainly been used for frequency discriminating power measurements like intermodulation distortion. They are also used for measurements of modulated signals. They are slower but provide higher dynamic range (>100dB) than power meters. Accuracy for relative measurements is good but normally inferior to power meters for absolute measurement of power. In combination with demodulation (signal analyzers) it is the main tool for base-band signal analysis and a main component for future systems where load-pull is combined with in-band distortion modeling.

Vector Network Analyzers

Systems based on VNA were traditionally limited to CW and harmonic measurements using receiver mode. The dynamic range is excellent (>100 dB) and the impedances can be monitored during measurement. Therefore VNA was normally used in combination with active loads, [82]. Recent systems have been using the VNA as a general receiver. Using up-conversion it is now even used for envelope impedance measurements [79]. A VNA is also used in a power-meter based system. Both for calibration and for phase distortion measurements (AM to PM conversion).

Time Domain

An alternative receiver used in many university systems was the Microwave Transition Analyzer, MTA. This was a time-domain sample based high frequency instrument with advanced vector correction. It is no longer available on the market. It has now been replaced by large-signal network

analyzers, LSNA, capable of analyzing modulated signals in time-domain with advance calibration features, [90]. It is likely that these systems together with sampling oscilloscopes will play a more important role in load-pull in the future, [91]. This is mainly due to the increased bandwidth in modern telecom systems.

4.2.4 Typical System Configurations

Single-tone, CW, Power Characterization

The typical power-meter based continuous wave load-pull system for on-wafer measurements that was used in this work is shown in figure 4.29.

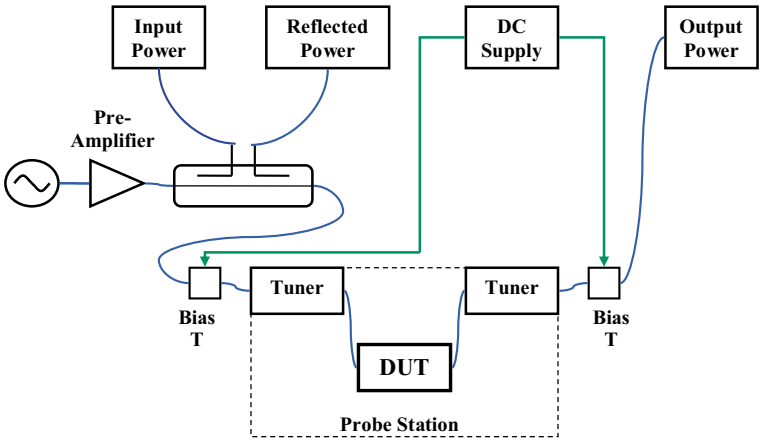

Fig. 4.29. Load-pull system for on-wafer CW measurements.

It is based on a Maury Microwave automated tuner system, ATS. Input power, reflected power and output power were measured using power meters with diode-based high-dynamic range sensors. The tuners were pre-calibrated in about 8000 points with a VNA using through-reflect-line, TRL calibration which is the most accurate for high Γ measurements. No de-embedding for the wafer test-connection was used for the load-pull measurement. Harmonics impedances were measured but not controlled. The system was calibrated using the build in Maury ATS power calibration algorithm with source match calibration, [92]. The probe-station was calibrated as if it was a test-fixture extracting the response as the difference between a line-reflect-match, LRM, or a short-open-load-through, SOLT on-wafer calibration and a coax SOLT calibration at the probe station interface [49]. Results from continuous wave load-pull measurements are presented in [paper-I], [paper-II] and as reference in [paper-VIII].

Two-tone Power Characterization

Intermodulation measurements are conducted using a two-tone setup as shown in figure 4.30.

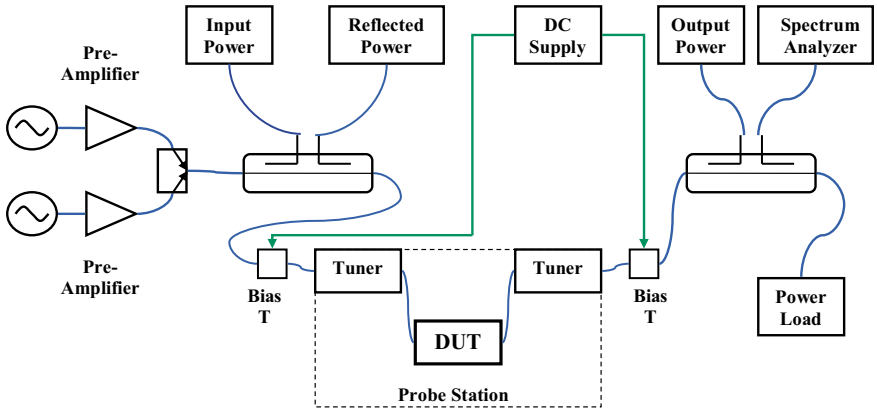

Fig. 4.30. Load-pull system for two-tone intermodulation distortion measurements.

In this work two separate analog signal generators were used with individual amplifiers for improved IMD measurements [93]. In addition to the normal load-pull calibration a system calibration of the relative spectrum analyzer levels was also done. Results from two-tone load-pull measurements are presented in [paper-I]-[paper-IV] and as reference in [paper-VIII].

Modulated Measurements

Modulated measurements can be conducted using the same setup as for the two-tone measurements by replacing the two generators with a single generator with IQ-modulator. A base-band generator creates the modulated signals. Two-tone or multi-tone investigations can be conducted in the same setup by generating the multi-tones digitally but it will require a very linear pre-amplifier not to cause severe problems with intermodulation distortion in the input signal to the DUT [93].

Load-Pull with Bias-Modulation

In [paper-VIII] a load-pull system for device evaluation under varying bias conditions was suggested and evaluated. The system is based on using a power-analyzer to replace the normal fixed-bias and provide the varying drain supply-voltage [94]. The amplitude modulation is created by two CW signal generators, phase controllable and with certain tone spacing. A drain bias control-signal based on the created AM envelop is computed from a modulator model and down-loaded into the power-analyzer. The bias system is calibrated using peak-power envelope synchronization described in detail in [paper-VIII]. A system outline is shown in figure 4.31.

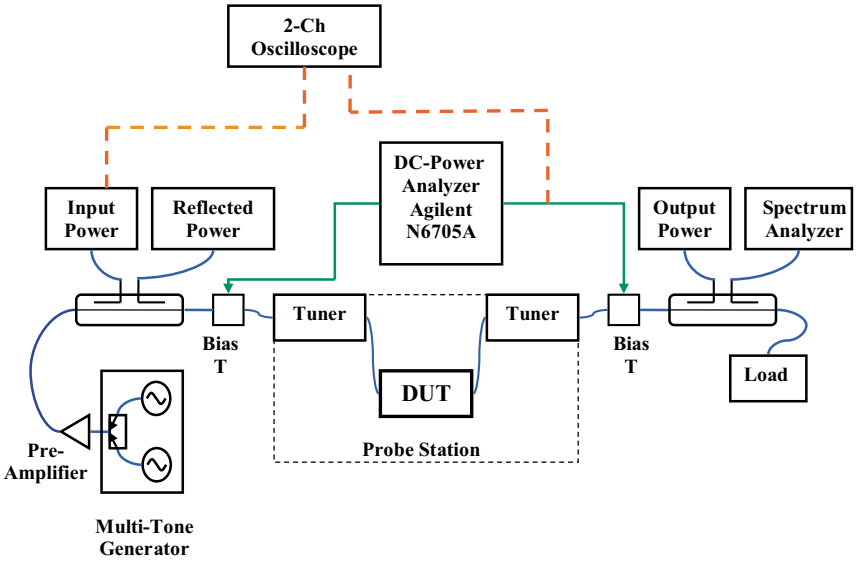

Fig. 4.31. Load-pull system for bias-modulated measurements.

Compared to modern wideband signals the system has very low modulation bandwidth of about 1 kHz. Nevertheless it is a first attempt to conduct actual bias modulated measurements at device level. The main bandwidth limitation in the system is the power-analyzer. The concept will with few modifications be applicable also for improved bandwidth systems for digital modulation (see 4.2.6 future work).

4.2.5 Accuracy in Load-Pull Measurements

There is a general concern of accuracy in large-signal characterization of microwave power devices, [76]. It is sometimes found that a device measured in one laboratory shows different results in another. This is probably due to inconsistency in one or more of the parameters specified in figure 4.3. Therefore much work is now conducted in the measurements community to improve and standardize large-signal measurements procedures, [95].

In load-pull systems specifically there are inaccuracies related to the impedance measurement and to the power measurements. They largely depend on how the system is calibrated and what instruments are used. For the load-pull system used in this work the main errors are:

- tuner calibration errors
- repeatability of impedance positions
- break apart errors from tuner calibration
- errors from system component measurements
- instrumentation inaccuracies

They have been minimized by using optimum calibration methods, highly repeatable connectors and optimum instrument setting during measurements. The actual impedance error can be estimated by measuring the impedance seen looking into the loads in different positions from a calibrated probe interface. The error in Γ in the measurements in this work was usually less than ±0.02 ∠ ±2°. The overall system accuracy can also be estimated by measuring gain difference versus impedance for a through-line [96].

4.2.6 Future Work

Future work involves modifying the load-pull method to be able to fully characterize RF- power transistors for new high-efficient operating modes. This involves adapting the bias modulated system for higher bandwidths using an arbitrary waveform generator, AWG, with an envelope amplifier to create the bias-modulation signal as shown in figure 4.32.

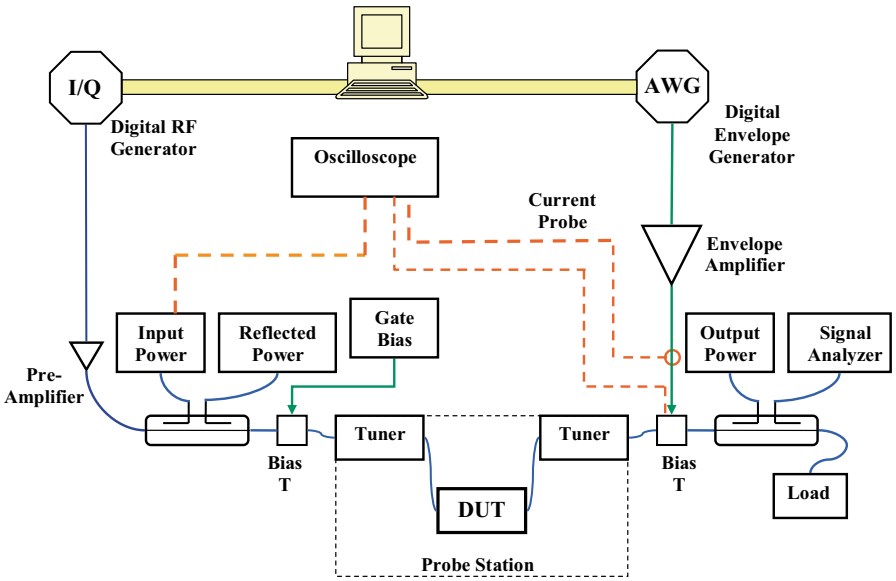

Fig. 4.32. Load-pull system for bias-modulated measurements.

The bias-tees need to be modified for higher cut-off frequency. LF supply power is monitored though the current probe and voltage measurement with the oscilloscope.

4.3 Load-Pull Summary with Results

Two new methods for computational load-pull of RF-power components for high-efficiency PA-systems have been implemented and tested. CLP simulations have shown that the main factors affecting the 5 % increase in efficiency for the LDMOS transistor in class-F are the reduced power dissipation in the device due to a reduced charging-discharging current for the output capacitance and the increased output-power at the fundamental frequency due to class-F waveform shaping [paper-VII].

The CLP investigation with bias-modulation show a 10-15 % increase in efficiency in the mid-power range for the selected modulator model for the LDMOS transistor [paper-V]. This is in the same range as the results measured on the fabricated device using the novel load-pull measurement configuration presented in [paper-VIII].

The CLP investigation of LDMOS on SOI clearly shows that low resistivity and high resistivity substrates are superior for RF-power with regards to efficiency. They show 10 % higher drain-efficiency in the RF-range. The investigation also shows that much information about the frequency dependency for RF-power applications can be identified also from small-signal on-state simulations. Since the simulations have been conducted on a 2D structure it has been possible to make a model of the transistor output based on the optimum load-line match [15]. This model shows almost identical values for the output capacitance as the on-state small-signal simulations [paper-VII].

5. Concluding Remarks

Silicon LDMOS transistors are and will continue to be the mainstream technology for power amplification at radio frequencies in a foreseeable future. Despite new materials with superior properties for the application the mature silicon technology provides the most cost-effective solution.

Albeit the technology is mature much work still remains to fully optimize the LDMOS technology for modern PA applications. Distortion produced is today handled by external circuitry at the expense of overall system efficiency and in the end cost. Much work is therefore today conducted in the field of efficiency-enhancement.

Much is known about the distortion mechanisms on device level but most of the work is based on circuit modeling sometimes distant from the physics of the device design and processing. TCAD has been used for many years for technology and device development but more work remains to develop the tools for nonlinear-analysis at device level. This work has shown that TCAD can be used for the understanding of transistor behavior under high-efficiency operating conditions. Based on this work it is plausible that the nonlinear mechanisms of the LDMOS in the future can be better understood using TCAD simulations without the need of circuit modeling. It will also be possible to optimize devices for different modes of operation, including efficiency-enhancement techniques like envelope-tracking, prior to fabrication.

Summary of Papers

5.1 Paper I

Novel BiCMOS Compatible, Short Channel LDMOS Technology for Medium Voltage RF & Power Applications

A novel BiCMOS compatible medium voltage LDMOS transistor is presented. The p-well is shaped using only an angular implantation creating a channel length of approximately 0.15 μm. The extended drain drift region is covered by a thick field oxide reducing the gate-drain capacitance and increasing the breakdown voltage. DC small-signal and load-pull power response are explored of the shortest, 1.0 μm, drift region length device. It is shown to have an f_T, of 13 GHz and an f_{MAX} of 27 GHz. At 1900 MHz with 12 V supply voltage it produces 20 dB gain and a 100 mW output power. The drain efficiency is 43% at the 1 dB compression point for a maximally flat gain at a quiescent drain current of 3 mA. The power possibility with the technology is investigated by higher frequency load-pull power measurements at 2.45 GHz and 3.0 GHz. The non-linear response is also measured using two-tone load-pull measurements showing third order intermodulation products of about -20 dBc at 1900 MHz at a peak envelope power of 21 dBm.

The author's contribution to this paper was all process and device simulations, all small-signal and load-pull measurements and the writing related to those parts.

5.2 Paper II

Small Signal and Power Evaluation of Novel BiCMOS Compatible, Short Channel LDMOS Technology

The previously described angular implanted medium voltage LDMOS technology is explored in more detail. The relationship between the drain drift region length and the breakdown voltage of the technology is studied for the different drift region lengths, 1.0 μm, 1.5 μm and 2.2 μm. f_T and f_{MAX} are studied under different bias conditions for the different structures and the

bias dependency of the input capacitance is computed from the transconductance and f_T using the simple first order general FET model. The input capacitance in shown to be strongly bias-dependent and up to three times the oxide capacitance. The drain drift region is shown to have a minor 10 % impact on f_T but an almost 40% impact on f_{MAX} and the reasons for this are discussed in the paper. In the paper the technology is also studied under different drain voltage conditions. It is found that f_{MAX} increases with drain bias and f_T decreases. This is credited to the reduced output capacitance with increased drain voltage.

The author's contribution to this paper was all process and device simulations, all small-signal and load-pull measurements, part of the analysis and the writing related to those parts (major part).

5.3 Paper III

Investigation of the non-linear input capacitance in LDMOS transistors and its contribution to IMD and phase distortion

In this paper the different contributions to the mechanisms of the nonlinear bias-dependent input capacitance of RF-Power LDMOS transistors is explored using TCAD. Simulated data is compared to data extracted from high frequency measurements for verification. An analysis is first made at 0 V, outlining the contribution of the individual terminal capacitances to the nonlinear input capacitance. This is followed by an on-state high-field analysis. Finally the capacitance behavior under power-match conditions is explored based on load-line matched conditions. The input capacitance along the transfer function is extracted and analyzed. It is found that this capacitance function is very load dependant and more non-linear studied over a load-line. The impact of the non-linear capacitance has on phase distortion is also explored. Using computational load-pull simulations it is found that the on-set of phase-distortion is closely correlated with the entry into a very non-linear capacitance region of the input capacitance.

The author's contribution to this paper was part of the planning, all device simulations, small-signal measurements, part of the small-signal analysis, major part of the large-signal analysis and major part of the writing.

5.4 Paper IV

A Method for Device Intermodulation Analysis from 2D, TCAD Simulations using a Time-domain Waveform Approach

A method for intermodulation analysis based on TCAD simulations is presented. A load-line transfer function is simulated using parasitic drain resistance in the TCAD simulation. The drain current versus gate voltage is simulated over an optimum class-A resistance on the drain. A two-tone time-domain signal is generated and a look-up table with the transfer-function data is used to create the output current waveform. The time limited series is filtered and an FFT is used to produce the spectral output of the transistor. The results are presented as IM3, IM5 and IM7 versus input voltage. In the paper the results are compared to load-pull, two-tone measurements of a similar fabricated device and the method is shown to provide qualitatively good results for an initial comparative intermodulation distortion analysis at an early stage in the device design process.

The author's contribution to this paper was the idea and planning, all device simulations, algorithm implementation, all large-signal measurements and major part of the writing.

5.5 Paper V

A Computational Load-Pull Method for TCAD Optimization of RF-Power Transistors in Bias-Modulation Applications

Envelope-tracking is a method of efficiency enhancement that looks promising for the future. For LDMOS transistors with a considerable output capacitance optimum matching under varying drain-bias conditions vary. In this paper a method is presented that enables device analysis under varying drain bias in TCAD. A two-tone signal creates a varying envelope time-domain signal. A voltage source on the drain is correlated to the envelope of the input signal with amplitude computed from a modulator model. Large-signal time-domain simulations are then conducted under optimum impedance match conditions to find the response of the circuit. The response is compared to an identical setup without bias modulation. It is found that drain bias-modulation can increase the drain-efficiency about 15 % in the mid-power region.

The author's contribution to this paper was the idea and planning, all device simulations, algorithm implementation and major part of the analysis and writing.

5.6 Paper VI

A Computational Load-Pull Method with Harmonic Loading for High-Efficiency Investigations

In class-F amplifiers open-circuited odd harmonics create a square-waved voltage waveform favorable for high efficiency operation. In this paper a computational load-pull method for harmonic impedance tuning is explored. The method is based on using active loads for harmonic tuning in combinations with passive load for the fundamental component. With this method a normal class-AB simulation is compared to an improved efficiency class-F simulation. From a time domain wave-form analysis the two main contributions to the increased efficiency are identified, the 9 % increase in output power at the fundamental component due to waveform clipping and the 17 % reduced losses in class-F in the charging-discharging of the output capacitance.

The author's contribution to this paper was the idea and planning, all device simulations, algorithm implementation and major part of the analysis and writing.

5.7 Paper VII

Investigation of SOI-LDMOS for RF-power applications using Computational Load-Pull

Previous work has indicated that substrate resistivity for SOI-LDMOS is an important factor to consider for RF-power design on SOI. It has been shown that if off-state output resistance can be considered to correlate with high efficiency then a medium resistivity substrate is a poor choice for LDMOS design on SOI. In this paper computational load-pull is used to make a more detailed efficiency analysis of SOI-LDMOS. It is found that low resistivity substrate or high resistivity substrate give a 10 % increase in drain-efficiency. The reason for the lower efficiency for the medium resistivity substrate is the combination of a high output capacitance due to lack of depletion under the buried oxide and fairly high series resistance in the charging-discharging of the output capacitance. The optimum load impedance found from computational load pull also shows that the output capacitance necessary to compensate for under large signal operation correlates well to the on-state capacitance. Therefore conclusions can be made form the on-state small-signal simulations about frequency decency of high efficiency in large-signal operation.

The author's contribution to this paper was part of the small-signal analysis, major part of the large-signal analysis and modeling and major part of the writing.

5.8 Paper VIII

A Novel Load-Pull Configuration for Envelope Tracking Applications

Device characterization for RF-power device design is normally conducted using load-pull measurements. For characterization under drain bias-modulation it has been necessary to first build an amplifier and then study it under drain-bias modulation. In this paper a load-pull measurement setup is presented where narrow band drain-bias modulations is possible under varying load impedance conditions. A modulator model for high efficiency operation is first extracted from continuous wave load-pull measurements under varying drain-bias conditions. A modulation drain-bias waveform based on a two-tone envelope is then calculated and downloaded into a power analyzer acting as time varying voltage supply in the load-pull setup. Calibration for the envelope-phase is conducted using peak-power correlation. The method shows the expected 10-15 % efficiency increase in the mid-power range. Some limitations in the measurement setup are also explored together with possible improvements for increased bandwidth of the system.

The author's contribution to this paper was the idea and planning, all measurements, and major part of the analysis and writing.

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