Application Note:

HFAN-1.0

Rev 1; 4/08

Introduction to LVDS, PECL, and CML

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MAXIM

Maxim Integrated Products

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LVDS, PECL, and CML I/O Structures

1 Introduction

As the demand for high-speed data transmission grows, the interface between high-speed ICs becomes critical in achieving high performance, low power, and good noise immunity. Three commonly used interfaces are PECL (positive-referenced emitter-coupled logic), LVDS (low-voltage differential signals), and CML (current mode logic). When designing high-speed systems, people often encounter the problem of how to connect different ICs with different interfaces. To deal with this, it is important to understand the input and output circuit configurations of each interface for proper biasing and termination. This paper describes various ways of interconnecting between PECL, CML, and LVDS for high-speed communication systems, using Maxim products as examples.

2 PECL Interface

PECL originates from ECL but uses a positive power supply. The relatively small swing of the PECL signal makes this logic suitable for high-speed serial and parallel data links. First developed by Motorola, the PECL standard has long since gained popularity with the rest of the electronics industry.

2.1 PECL Output Structure

The PECL output structure is shown in Figure 1. It consists of a differential pair that drives a pair of emitter followers. The output emitter followers should operate in the active region, with DC current flowing at all times. This increases switching speeds and helps maintain fast turn-off times. The proper termination for a PECL output is 50Ω to (V_{CC}–2V). At this termination, both OUT+ and OUT- will typically be (V_{CC}–1.3V), resulting in a DC current flow of approximately 14mA. The PECL output impedance is low, typically on the order of (4-5)Ω, which provides superior driving capability. When PECL outputs drive a transmission line, this low output impedance, which generates a mismatch in back termination, can result in high-frequency aberrations.

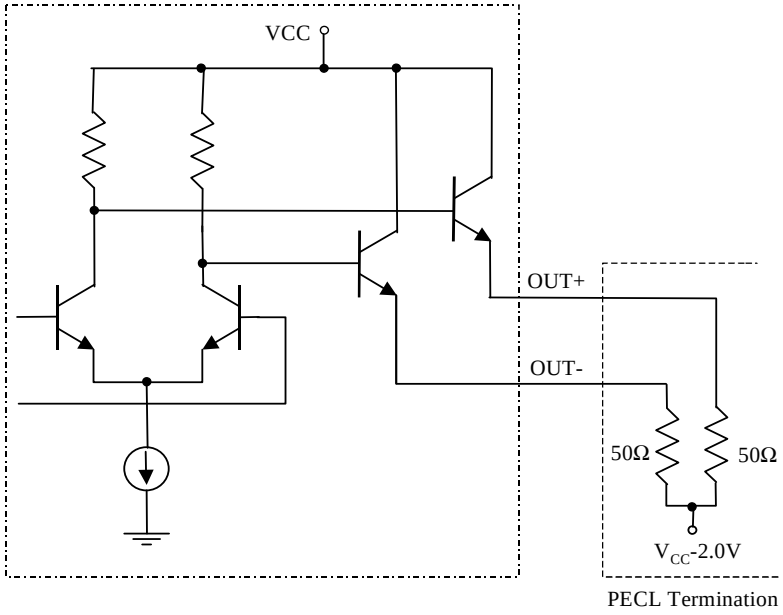


Figure 1. PECL output structure

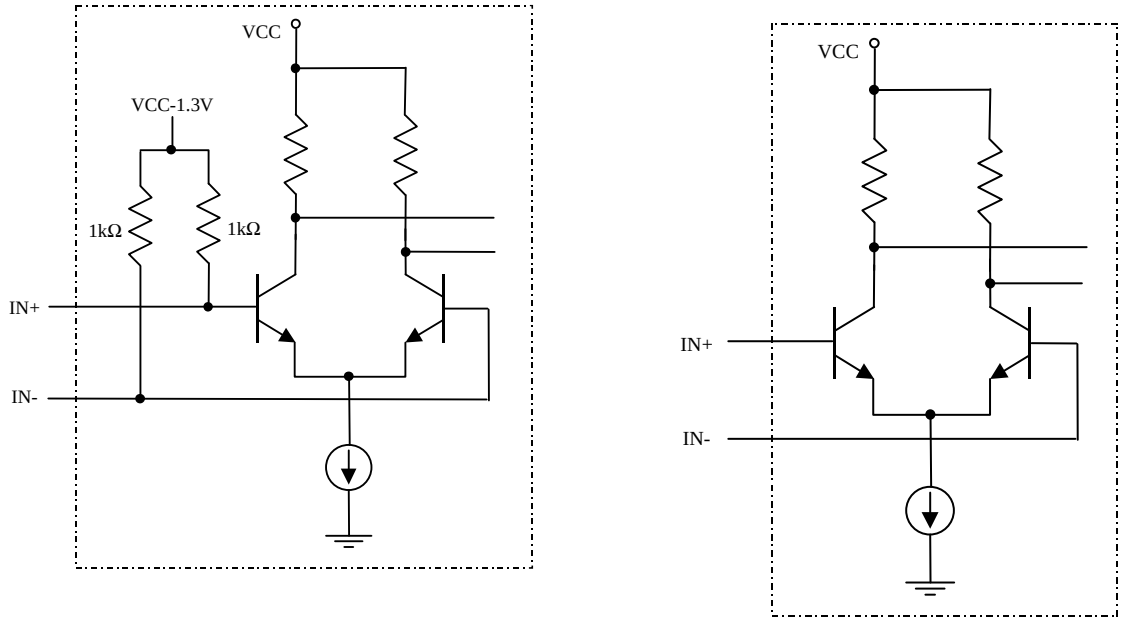
2.2 PECL Input Structure

The PECL input structure is shown in Figure 2. It is a current switching differential with high input impedance. In order to provide operating headroom, the common-mode voltage should be around (V_{CC}-1.3V). Maxim's HF communication products have two types of PECL input circuit configurations. One is with on-chip biasing (i.e., MAX3885); the other is without on-chip biasing (i.e., MAX3867, MAX3675). In the latter case, it is required that proper DC biasing be provided externally.

Table I gives Maxim's PECL input and output specifications.

The PECL interface is suitable for both +5.0V and +3.3V power supplies. When the power supply is +3.3V, it is commonly referred to as low-voltage PECL (LVPECL).

Careful attention must be paid to power-supply decoupling in order to keep the power-supply rail noise free. Also, the AC and DC requirements of the PECL outputs place additional constraints on termination networks.



(a) With on-chip high-impedance biasing

(b) Without on-chip biasing

Figure 2. PECL input structure

Table I. PECL Input and Output Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	T_A = 0°C to +85°C	V_{CC} – 1.025		V_{CC} – 0.88	V
	T_A = –40°C	V_{CC} – 1.085		V_{CC} – 0.88	V
Output Low Voltage	T_A = 0°C to +85°C	V_{CC} – 1.81		V_{CC} – 1.62	V
	T_A = –40°C	V_{CC} – 1.83		V_{CC} – 1.55	V
Input High Voltage		V_{CC} – 1.16		V_{CC} – 0.88	V
Input Low Voltage		V_{CC} – 1.81		V_{CC} – 1.48	V

3 CML Interface

CML is among the simplest protocols for high-speed interfacing. On-chip input and output terminations minimize the number of external components required to set the operating conditions. The signal swing provided by the CML output is small, resulting in low power consumption. In addition, the 50Ω back termination minimizes the back reflection, thus reducing high-frequency aberrations.

3.1 CML Output Structure

The CML output consists of a differential pair with 50Ω collector resistors, as shown in Figure 3. The signal swing is supplied by switching the current in a common-emitter differential pair. Assuming the current source is 16mA typical, and the CML output is loaded with a 50Ω pullup to V_{CC}, then the single-ended CML output voltage swings from V_{CC} to (V_{CC}–0.4V). In this case the CML output differential swing is 800mV typical and the common mode voltage is (V_{CC} – 0.2V). For the same source current, if the CML output is AC-coupled to 50Ω, the DC impedance is now set by the 50Ω collector resistor. The CML output common-mode voltage is now (V_{CC} – 0.4V), and the differential swing is 800mV_{p-p}. The output waveforms for AC- and DC-coupling are shown in Figure 4.

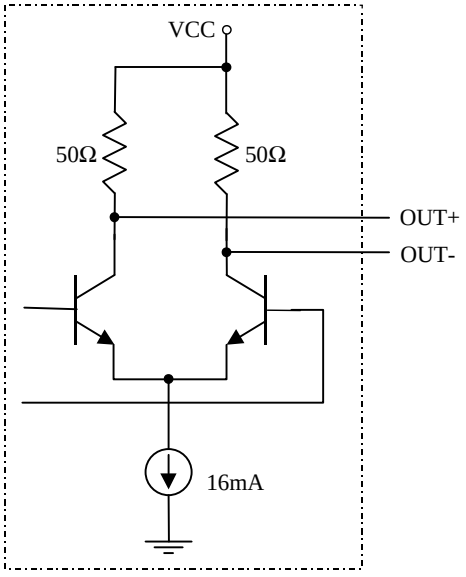


Figure 3. CML output structure

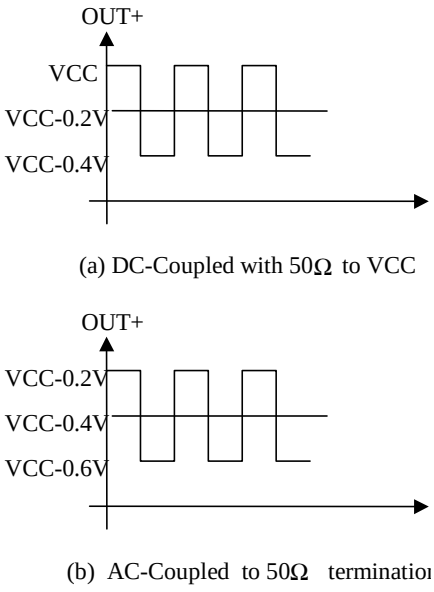


Figure 4. CML output waveform for DC- and AC-coupling

3.2 CML Input Structure

The CML input structure has several features that make it a popular choice for high-speed operations. As shown in Figure 5, Maxim's CML input structure has 50Ω input impedance for easy termination. The input transistors are emitter followers that drive a differential-pair amplifier.

Figure 5. CML input circuit configuration

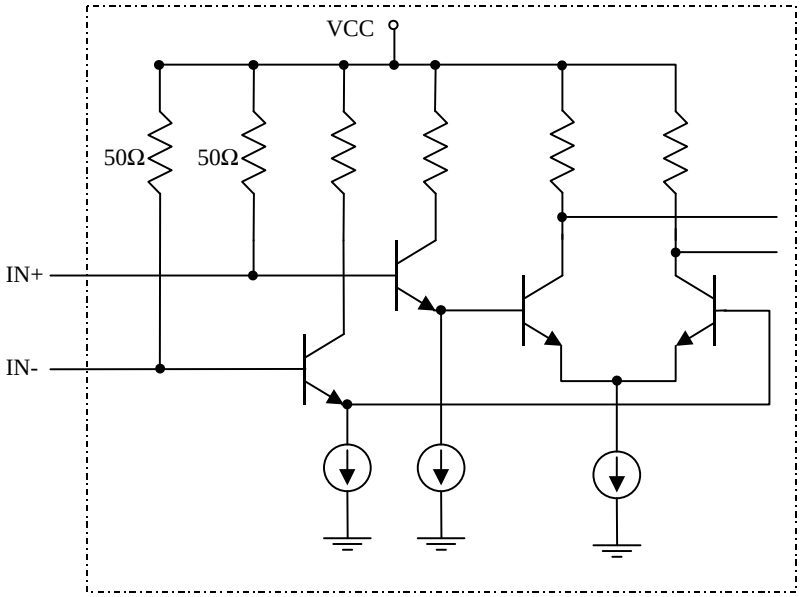


Table II lists the CML output and input specifications for the MAX3831/MAX3832.

Table II. CML Input and Output Specifications (Load = 50Ω to V_{CC})

PARAMETER	CONDITION	MIN	TYP	MAX	Units
Differential Output Voltage		640	800	1000	mV_{p-p}
Output Common Mode Voltage			V_{CC}-0.2		V
Single-Ended Input Voltage Range	V_{IS}	V_{CC} – 0.6V		V_{CC} + 0.2V	V
Differential Input Voltage Swing		400		1200	mV_{p-p}

Note: Different Maxim products have different CML input sensitivities (i.e., MAX3875, MAX3876).

4 LVDS Interface

LVDS is defined for low-voltage differential signal point-to-point transmission. It has several advantages that make it attractive to users. The low signal swing yields low power consumption, at most 4mA are sent through the 100Ω termination resistor. This makes LVDS desirable for parallel link data transmission. The signal levels are low enough in voltage to allow for supply voltages as low as 2.5V. Because the input voltage range is from 0V to 2.4V and the single-ended signal swing is 400mV, the input common-mode voltage will be from 0.2V to 2.2V. Therefore, LVDS can tolerate a ±1V ground potential difference between the LVDS driver and receiver.

4.1 LVDS Output Structure

Maxim's LVDS output structures are optimized for low-power and high-speed operation. The circuit configuration is shown in Figure 6. The differential output impedance is typically 100Ω. Refer to Table III for other output specifications.

4.2 LVDS Input Structure

The LVDS input structure, shown in Figure 7, has on-chip 100Ω differential impedance between IN+ and IN-. To accommodate a wide common-mode voltage range, an adaptive level-shifting circuit sets the common-mode voltage to a constant value at the input of a Schmitt trigger. The Schmitt trigger provides hysteresis relative to the input threshold. This signal is then applied to the following differential amplifier stage.

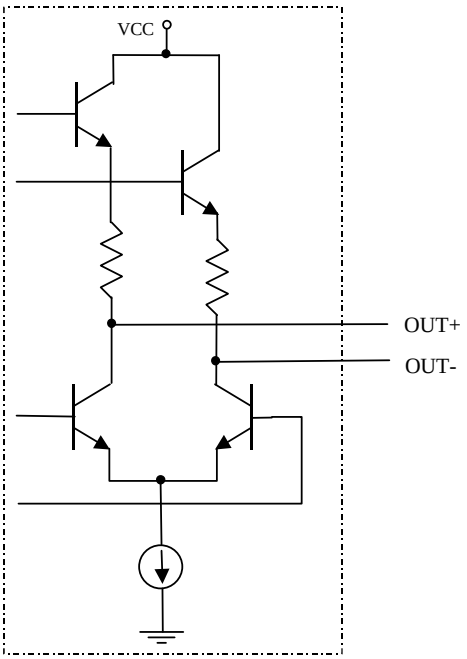


Figure 7. LVDS input structure

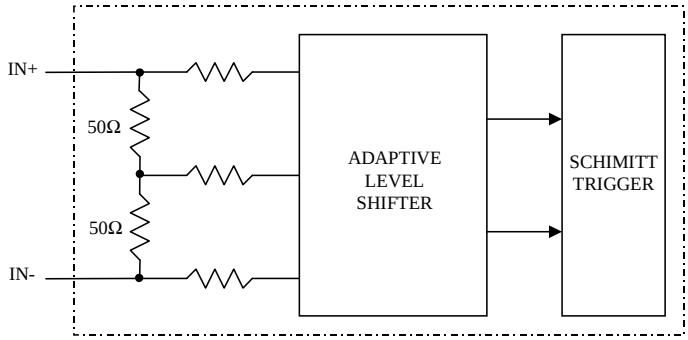


Table III summarizes Maxim's LVDS input and output specifications. (Applies to the MAX3831, MAX3832, and MAX3890.)

Figure 6. LVDS output structure

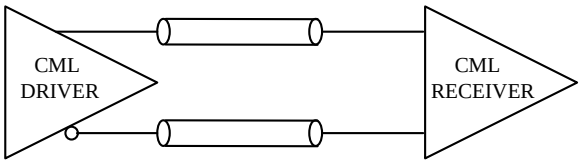
Table III. LVDS Input and Output Specifications

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	$\lvert V_{od} \rvert$		250		400	mV
Change in Magnitude of Differential Output for Complementary States	$\Delta\lvert V_{od} \rvert$				25	mV
Offset Output Voltage			1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	$\Delta\lvert V_{os} \rvert$				25	mV
Differential Output Impedance			80		120	Ω
Output Current		Short together			12	mA
Output Current		Short to GND			40	mA
Input Voltage Range	V_i		0		2.4	V
Differential Input Voltage	$\lvert V_{id} \rvert$		100			mV
Input Common-Mode Current		LVDS Input V_{OS} = 1.2V		350		µA
Threshold Hysteresis				70		mV
Differential Input Impedance	R_{in}		85	100	115	Ω

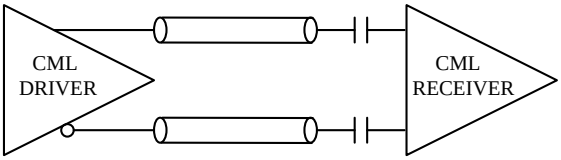
5 Mutual Interfaces

5.1 CML to CML

If the receiver and transmitter use the same supply voltage for V_{CC}, the CML driver output can be DC-coupled to the CML receiver input without additional components. AC-coupling can be used for systems in which the receiver and transmitter are at different supply voltages. For AC-coupling, the coupling capacitor should be large enough to avoid excessive low-frequency droop when the data signal contains long strings of consecutive identical digits (refer to application note HFAN-1.1). The CML to CML connection is given in Figure 8.



(a) DC-coupling between CML and CML



(b) AC-coupling between CML and CML

Figure 8. CML to CML interface

5.2 PECL to PECL

5.2.1 DC-Coupling: Thèvenin Equivalent of 50Ω to (V_{CC}-2V)

The PECL output is designed to drive a 50Ω load to (V_{CC} – 2V). Because the potential of (V_{CC} – 2V) is usually not available for termination networks, it is often preferable to find a parallel combination of resistors that result in a Thèvenin equivalent circuit. Figure 9 shows the result of the Thèvenin transformation. The termination requirement of 50Ω to (V_{CC} – 2V) imposes the conditions of $(V_{CC} - 2V) = V_{CC}\left(\frac{R2}{R1+R2}\right)$ and $(R1 // R2) = 50\Omega$. Solving for R1 and R2 yields the following

$$R1 = \frac{50 \cdot V_{CC}}{(V_{CC} - 2V)} \quad \text{and} \quad R2 = 25 \cdot V_{CC}$$

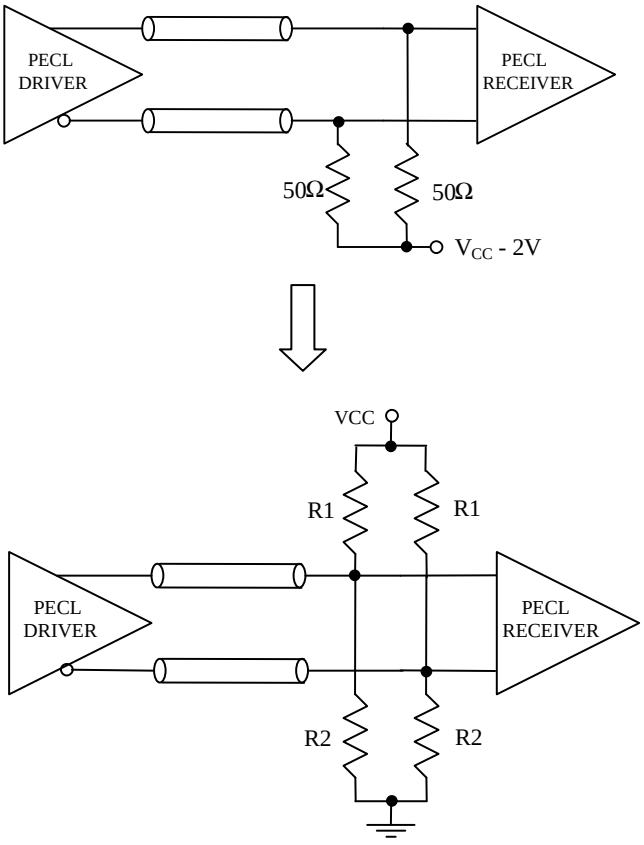


Figure 9. Thevenin equivalent transformation

At 3.3V, the standard 5% resistor values would be R1 = 130Ω and R2 = 82Ω. At +5.0V, the derived values would be R1 = 82Ω and R2 = 130Ω. Figure 10 gives the Thevenin equivalent termination networks for +3.3V suppy and +5.0V supply.

Note that PECL output configurations are open-emitter and have no back termination (see Figure 1).

5.2.2 AC-Coupling

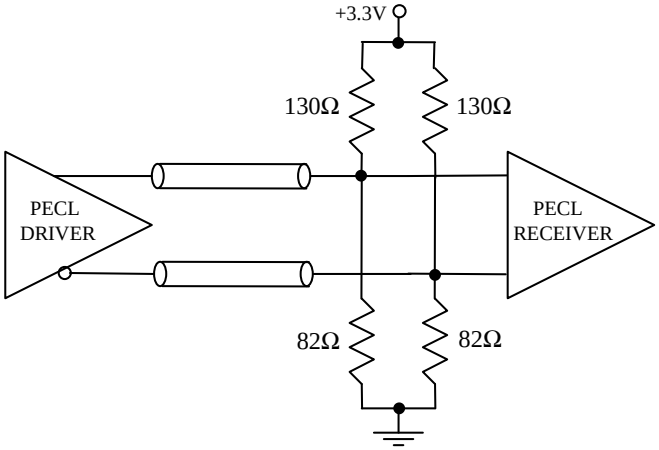
When PECL outputs need to be AC-coupled to a 50Ω termination, a resistor to ground should be used to DC-bias the PECL output before AC-coupling to the transmission line, as shown in Figure 11.

For a PECL input termination R2 and R3 should be selected by considering the following: (1) PECL input DC bias voltage should be set at (Vcc-1.3V); (2) matching the characteristic impedance of the transmission line; (3) power consumption; and (4) external component count. Fig. 11(a) optimizes for the lowest number of components. In this case R2 and R3 are determined by $\frac{R3 \cdot Vcc}{R2 + R3} = Vcc - 1.3V$, and $R2 // R3 \approx 50\Omega$. This results in:

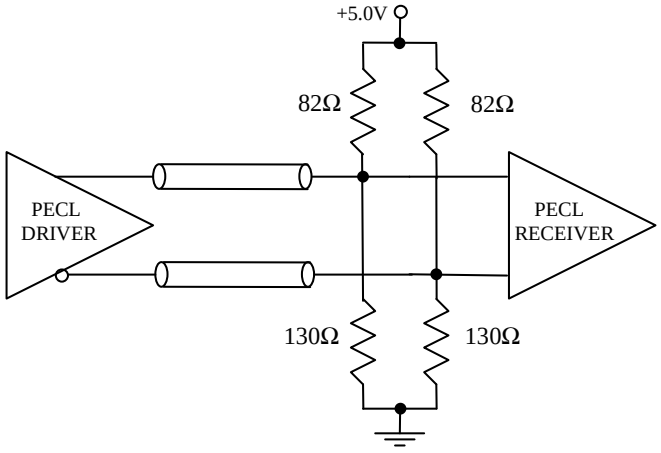
R2 = 82Ω and R3 = 130Ω for +3.3V supply

and

R2 = 68Ω and R3 = 180Ω for +5.0V supply

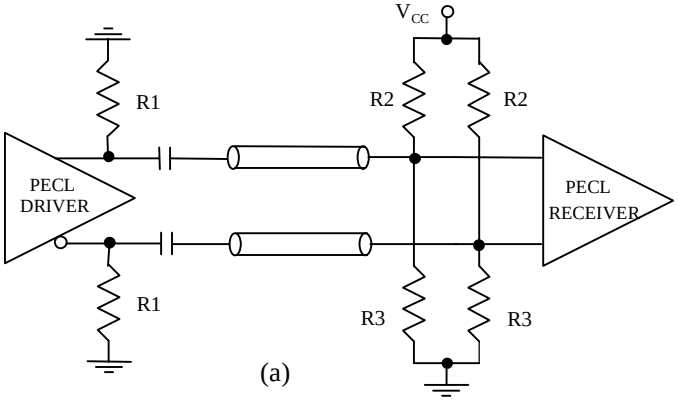


(a) 3.3V supply



(b) 5.0V supply

Figure 10. DC-coupling between PECL and PECL



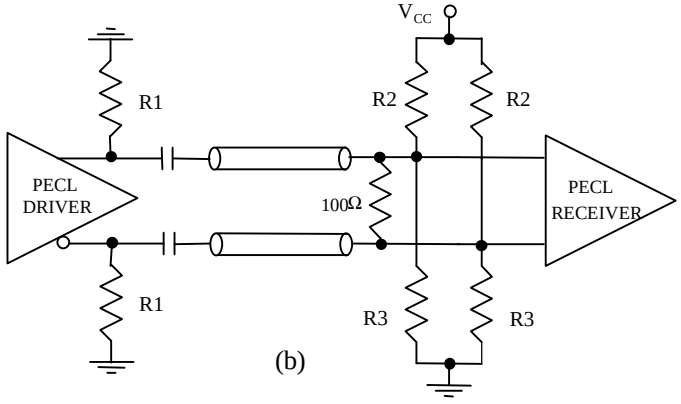


Figure 11. AC-coupling between PECL and PECL

The disadvantage of Figure 11(a) is that the power consumption caused by this termination network is high. For systems where power consumption is a main concern, Figure 11 (b) can be used. In this case we need to make $\frac{R3 \cdot Vcc}{R2 + R3} = Vcc - 1.3V$, and $R2 // R3 // 50\Omega = 50\Omega$.

One solution is this

R2 = 2.7kΩ and R3 = 4.3kΩ for +3.3V supply

and

R2 = 2.7kΩ and R3 = 7.8kΩ for +5.0V supply

Because the PECL output common-mode voltage is fixed at (V_{CC}-1.3V), the DC-biasing resistor (R1) can be selected by assuming a 14mA DC current. An initial calculation would be $R1 = (Vcc - 1.3V)/14mA$, resulting in R1=142Ω for +3.3V supply and R1=270Ω for +5.0V supply. However, this calculation gives less than 50Ω AC termination resistance as seen from the PECL output. In real applications to balance both the AC and DC requirements, R1 can be selected between 142Ω and 200Ω for a +3.3V supply and between 270Ω and 350Ω for a +5.0V supply.

Further improvement in PECL terminations can be achieved in two ways: (1) Add a resistor in series with the coupling capacitor such that the AC impedance seen by the PECL driver is close to 50Ω, (2) place an inductor in series with R1, which allows the AC impedance to be dominated by the receiver impedance and not by R1.

5.3 LVDS to LVDS Interface

Because the LVDS input has on-chip terminations, the interface between LVDS driver to LVDS receiver is simply a direct connection, as shown in Figure 12.

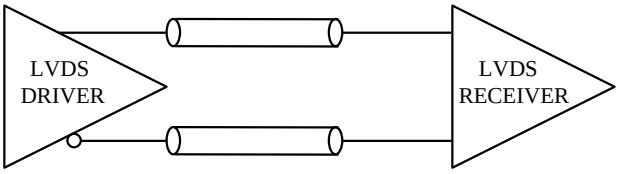


Figure 12. LVDS to LVDS interface

6 Interface between LVDS, PECL, and CML

In the following, +3.3V PECL is assumed.

6.1 LVPECL to CML

LVPECL to CML coupling can be accomplished using AC or DC methods.

6.1.1 AC-Coupling

One way to AC-couple an LVPECL driver to a CML receiver is shown in Figure 13. On each of the LVPECL outputs, a resistor R (142Ω to 200Ω) can be connected to ground for proper DC biasing. If the LVPECL differential output swing is larger than what the CML receiver can handle, a 25Ω series resistor can be used to provide a voltage attenuation of 0.67.

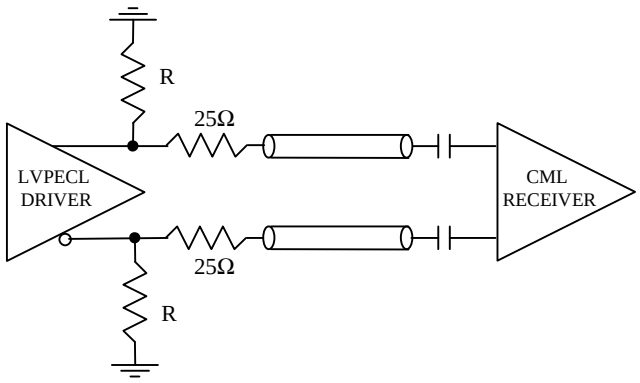


Figure 13. AC-coupling between LVPECL and CML

6.1.2 DC-Coupling

To perform DC-coupling between LVPECL and CML, a level shift network is needed to meet the common-mode voltage requirement at both the LVPECL output and the CML input. The attenuation introduced by this level shift network must be small so that the signal swing at the input of the CML receiver is above the receiver sensitivity. In addition, the total impedance seen from the LVPECL output should be kept close to 50Ω for impedance matching. The following example shows how to use an LVPECL output to drive the MAX3875 CML input. In this case the level shift network can be built as shown in Figure 14.

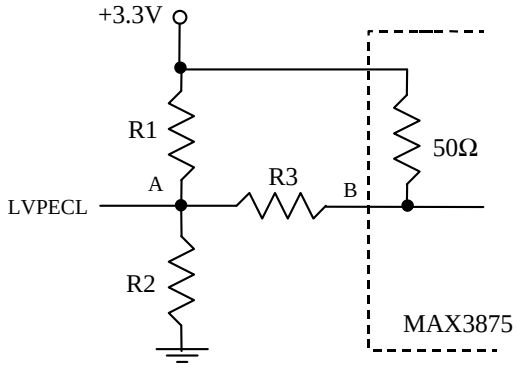


Figure 14. Resistor network between LVPECL and CML (MAX3875)

The following conditions need to be met:

$$V_A = V_{CC} - 2.0V = \frac{R2 \cdot Vcc}{R2 + R1//(R3 + 50\Omega)}$$

(1) [Open circuit Thevenin equivalent voltage]

$$Zin = R1 // R2 //(R3 + 50\Omega) = 50\Omega$$

(2) [Thevenin equivalent resistance]

$$V_B = V_{CC} - 0.2V = \frac{Vcc \cdot R3 + 50\Omega \cdot (Vcc - 1.3V)}{(50\Omega + R3)}$$

(3) [Assuming $V_A = V_{PECL\text{-}CM} = (V_{CC}\text{-}1.3V)$]

$$Gain = \frac{50}{(R3 + 50)} \geq 0.042$$

(4)

(Note: Assuming the LVPECL output minimum differential swing is 1200mV, and the MAX3875 has a input sensitivity of 50mV, the gain should be greater than 50mV/1200mV = 0.042.)

By solving the above equations, we obtained R1 = 182Ω, R2 = 82.5Ω, and R3 = 294Ω (standard 1% values). The resulting V_A = 1.35V, V_B = 3.11V, gain = 0.147, and Zin = 49Ω. When Connecting the LVPECL output to the MAX3875 input through this network, the measured V_A = 2.0V and V_B = 3.13V.

The DC-coupling between LVPECL and MAX3875 is shown in Figure 15. For other CML inputs, the minimum input common-mode voltage and minimum input swing can be different; therefore, the user can derive different resistor values based on the above considerations.

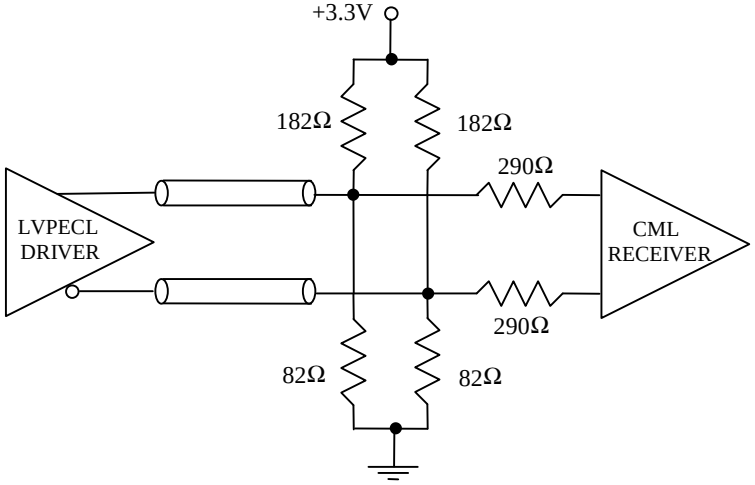
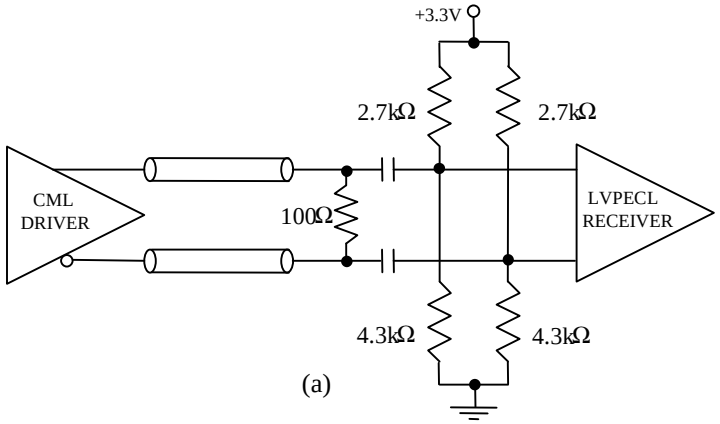
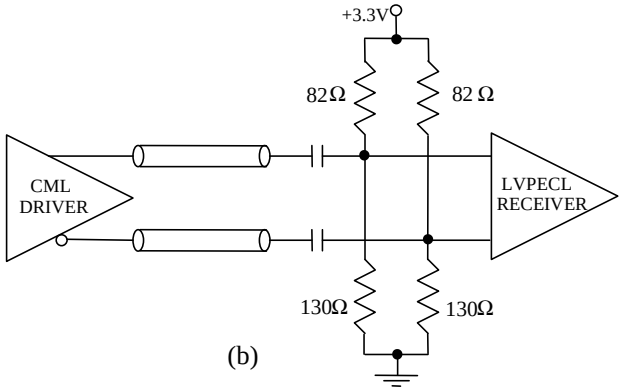
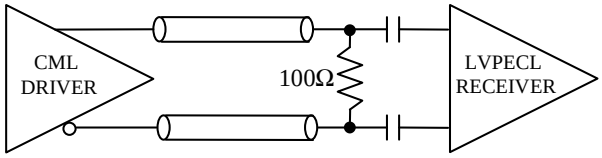


Figure 15. DC-coupling between LVPECL and CML (MAX3875)

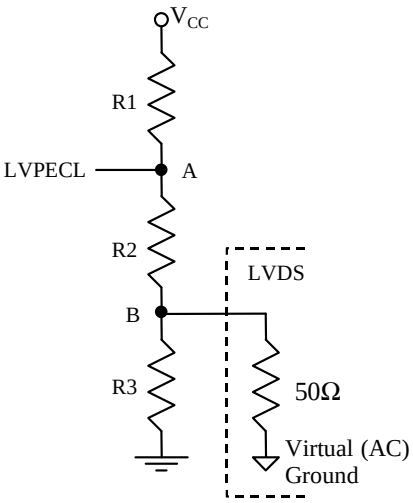




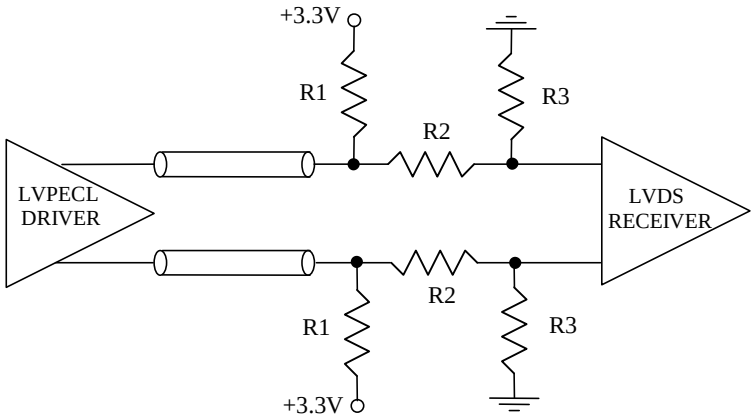


(c) LVPECL with on-chip high-impedance biasing

Figure 16. AC-coupling between CML and LVPECL



(a) Single-ended equivalent circuit



(b) LVPECL to LVDS interface

Figure 17. DC-coupling between LVPECL and LVDS

6.2 CML to LVPECL

AC-coupling is required when interfacing from CML to LVPECL (see Figure 16).

6.3 LVPECL to LVDS

6.3.1 DC-Coupling

DC-coupling between LVPECL and LVDS requires a level shifting/attenuation network, shown in Figure 17. Several conditions must be considered. First, the LVPECL output is optimized for a 50Ω load to (V_{CC}-2V). Next, the network attenuation should be such that the LVPECL output signal after attenuation is within the LVDS input range. Note that the LVDS input impedance is 100Ω differential, or 50Ω to virtual ground on each line (Figure 7). This does not contribute to the DC termination impedance, but does contribute to the AC termination impedance. This means that the AC and DC impedance will always be different. Therefore, the following equations should be satisfied:

$$V_A = V_{CC} - 2V = V_{CC} \cdot \frac{R2 + R3}{R1 + R2 + R3} \quad (1)$$

$$R_{AC} = R1 // (R2 + (R3 // 50\Omega) = 50\Omega \quad (2)$$

$$R_{DC} = R1 // (R2 + R3) \approx 50\Omega \quad (3)$$

$$Gain = \frac{R3 // 50\Omega}{R2 + (R3 // 50\Omega)} \geq 0.17 \quad (4)$$

By letting V_{CC} = +3.3V and solving the above equations, we obtain R1 = 182Ω, R2 = 47.5Ω, and R3 = 47.5Ω. The calculated V_A = 1.13V, R_{AC} = 51.5Ω, R_{DC} = 62.4Ω, and gain = 0.337. When connecting the LVPECL output through this termination network to the LVDS input, the measured common-mode voltages are V_A = 2.1V and V_B = 1.06V. Assuming the minimum LVPECL differential output is 930mV, then the minimum voltage applied to the LVDS input is 313mV, which meets the LVDS input sensitivity requirement. On the another hand, if the maximum LVPECL differential output is 1.9V, then the maximum signal at the LVDS input is 640mV, which also meets the LVDS input specifications.

6.3.2 AC-Coupling

The AC-coupling solution between LVPECL and LVDS is shown in Figure 18. The LVPECL output is DC-biased through a resistor R (142Ω to 200Ω) to ground. A 50Ω series resistor is necessary to attenuate the LVPECL output signal to satisfy the LVDS input requirement. At the LVDS input, a 5.0kΩ resistor to ground on each side is used to bias the common-mode voltage.

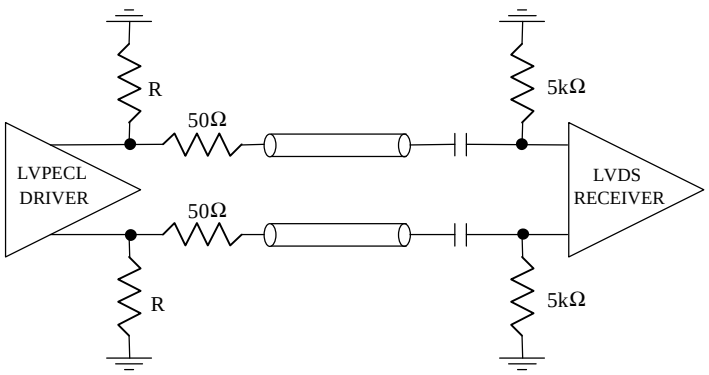


Figure 18. AC-coupling between LVPECL and LVDS

6.4 LVDS to LVPECL

A number of considerations should be made when using DC- and AC-coupling of LVDS to LVPECL

6.4.1 DC-Coupling

When DC-coupling between LVDS and LVPECL, use the resistor network shown in Figure 19. This resistor network shifts the DC level from the LVDS output (1.2V) to the LVPECL input (Vcc-1.3V). Because the LVDS output voltage is referenced to ground and the LVPECL input voltage is referenced to Vcc, this level shift network should be built so that the LVDS output is not sensitive to power-supply variations. Another important consideration is to make a trade-off between power consumption and speed. If we choose lower resistor values for (R1, R2, R3), the time constant formed by this resistor network and the LVPECL input parasitic capacitance is small, allowing for high-speed operation. On the other hand the total power consumption will be increased because more current will flow through these resistors. In this case the LVDS output performance can be affected due to power-supply variations. Again, the impedance

matching and network attenuation should be considered. The resistor values can be derived from the following equations:

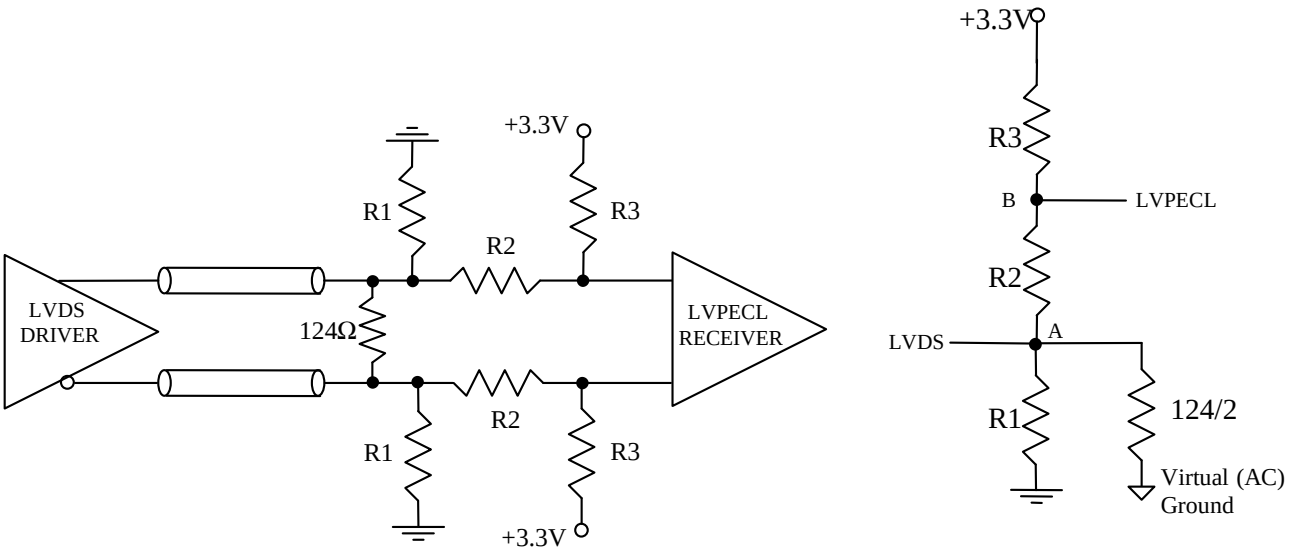
$$V_A = Vcc \cdot (\frac{R1}{R1+R2+R3}) = 1.2V \quad (1)$$

$$V_B = Vcc \cdot (\frac{R1+R2}{R1+R2+R3}) = Vcc - 1.3V \quad (2)$$

$$R_{IN} = (\frac{R3 \cdot (R1+R2)}{R3+(R1+R2)}) // 62\Omega = 50\Omega \quad (3)$$

$$Gain = \frac{R3}{(R2+R3)} \quad (4)$$

By applying V_{CC} = +3.3V and solving the equations above, we choose R1 = 374Ω, R2 = 249Ω, and R3 = 402Ω. This results in V_A = 1.2V, V_B = 2.0V, and R_{IN} = 49Ω, and gain = 0.62. Because the minimum LVDS output is 500mV$_{P-P}$ differential, the signal swing at the LVPECL input becomes 310mV $_{P-P}$. This voltage swing might be small for the PECL input standard, but most of the Maxim LVPECL input can accept this signal swing because of the high input amplifier gain. In a real application, the user needs to make a decision based on performance requirements.



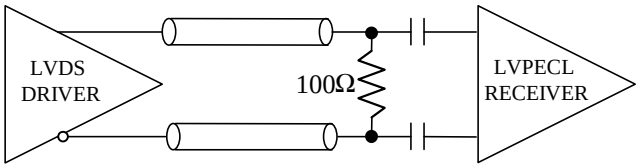
(a) LVDS to LVPECL interface

(b) Single-ended equivalent circuit

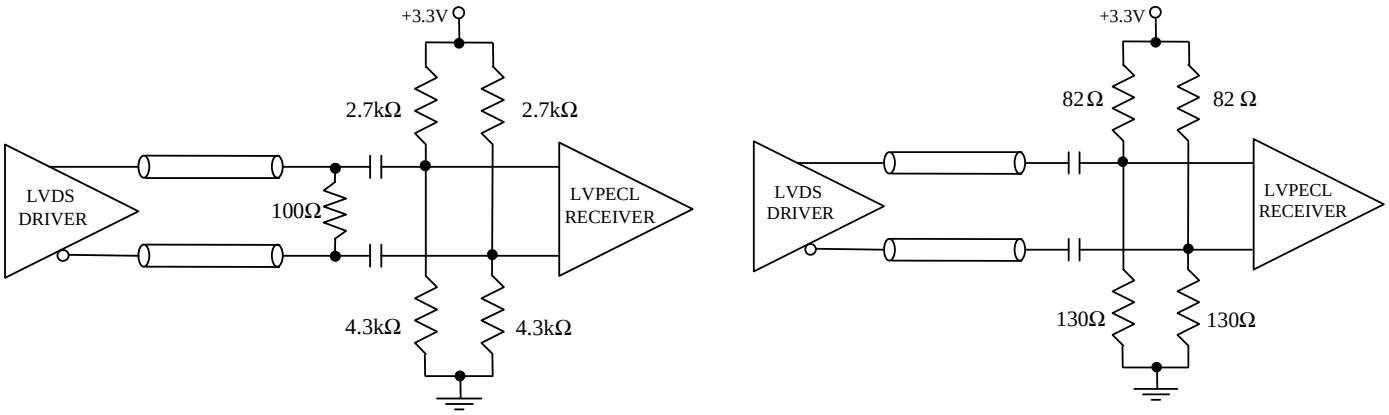
Figure 19. DC-coupling between LVDS and LVPECL

6.4.2 AC-Coupling

The AC-coupling between LVDS and LVPECL is simple, and two examples are given in Figure 20.



(a) LVPECL with on-chip termination (MAX3885)



(b) LVPECL without on-chip termination (MAX3867)

Figure 20. AC-coupling between LVDS and LVPECL

6.5 CML and LVDS Interfacing

Use AC-coupling when interfacing between CML and LVDS (Figure 21). Note that the CML output signal swing should be within the range that the LVDS input can handle.

If an LVDS driver needs to drive a CML receiver, the AC-coupling solution is given in Figure 22.

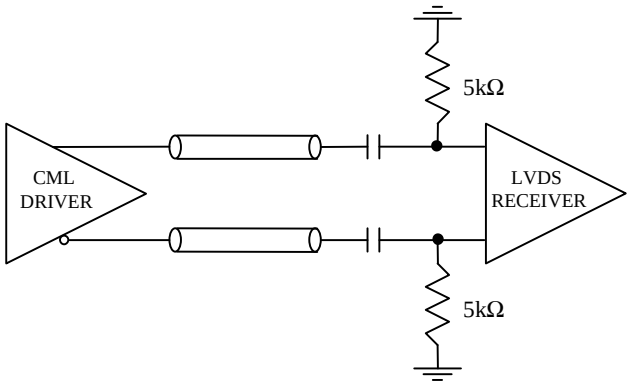


Figure 21. AC-coupling between CML and LVDS

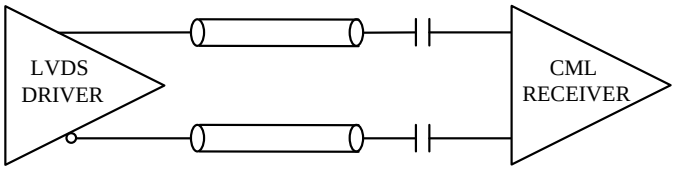


Figure 22. AC-coupling between LVDS and CML