ERICSSON TEI R&D Division
HW Department

Design object:

D.T.R.M. (Data Timing Recovery Module) based on an Injection Locked Oscillator

Technical description

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1 PREFACE

The simplest way to send data by a serial electrical link is to use two different physical connections: one for data and one for timing (clock). The second one can be avoided extracting the timing information from data by using a special code, for example CMI, HDB3, AMI, etc.
By using one of these transmission codes, the normal data bandwidth will be different distributed and some high frequency components will be generated. These components are used to extract the timing information. This procedure is called "Clock Recovery".
By using one of the previous code the data bandwidth will be enlarged. So, it will be necessary to increase the transmission media performance and consequently it will be more expensive.
This problem has been solved by using codes that preserve the bandwidth characteristics, but, in this case, the timing recovery operation is more difficult. In fact the circuits normally used for the clock extraction needs one or more data transitions every twelve bit group otherwise the clock could not be extracted. So, the code used must guarantee this condition.

Actually there are two methods to realize the clock extraction. The first consists of a PLL (Phase Locked Loop) circuit with a digital phase comparator that measure continuously the phase difference between the positive (or negative) data transition and the clock edge generated by a local oscillator. The frequency of this oscillator will be adjusted in order to have no phase difference between data and clock edges.
This is the most expensive solution because it is impossible to implement this circuit by discrete components. It must be realized by ASIC technology. Furthermore, there isn't any flexibility using this method because all of the physical parameters (frequency, pattern, etc.) cannot be changed to cover other possible requirements.

Another method, to extract the timing information, consists of the application of a Q Tank followed by an high gain selective amplifier stage. The Q Tank is realized by a simple LC circuit (or by using a SAW resonator) continuously stimulated from data edge transitions. This is a more flexible solution, but it has performances lower than the previous one. The clock recovered, for example, is affected by jitter because the S/N ratio is very low at the Q Tank output specially if the pattern used is poor of transitions.

In 1995 ERICSSON TEI has developed another type of timing recovery system using a new clock extractor called PCO (Pulse Controlled Oscillator). Detailed information about it will be shown in the present document.

2 GENERAL

2.1 Purpose

This document is the technical description of a new general purpose clock recovery circuit for telecommunication equipment. A particular clock extractor circuit (PCO) has been implemented for this application. Its description is contained in this document.

2.2 Overview

The circuit in object is developed in Ericsson TEI to find a possible alternative solution to extract the timing information from a 184.320 Mbit/s coded signal coming from an Optical or Electrical USI4 interface.

Our goal was to find a low cost and high performance solution to cover the requirements we have had for the US128K project.
Therefore we have started to investigate how it would have been possible to realize this solution having the following design pre-requisite: low cost, high performance, very small dimension, easy and fast implementation.
At the end of this analysis we have found a solution that cover all of the previous requirements.

The DTRM (Data Timing Recovery Module) is composed by four blocks contained into an hybrid circuit (41,2 mm x 10,6 mm). The packaging include a metal shield (virtually connected to the ground) to prevent electro magnetic irradiation. This circuit can operate in ECL or in PECL mode for optical or electrical link applications.

2.3 Abbreviations

DTRM	*Data Timing Recovery Module*
ECL	*Emitter Coupled Logic*
PCO	*Pulses Controlled Oscillator*
PECL	*Pseudo Emitter Coupled Logic*
PLL	*Phase Locked Loop*
STM1	*Synchronous Transfer Module (level 1)*
UIpp	*Units Interval (peak to peak)*
USI4	*Uni Switch Interface (level 4)*

3 FUNCTIONAL DESCRIPTION

3.1 Block Diagram

The DTRM block diagram is showed in fig. 3.1.1.
Four functional blocks are evidenced: a **Pulse Generator (PG)**, a **Clock Extractor (CE)**, a **Phase Aligner (PA)** and a **Clock Killer (CK).**

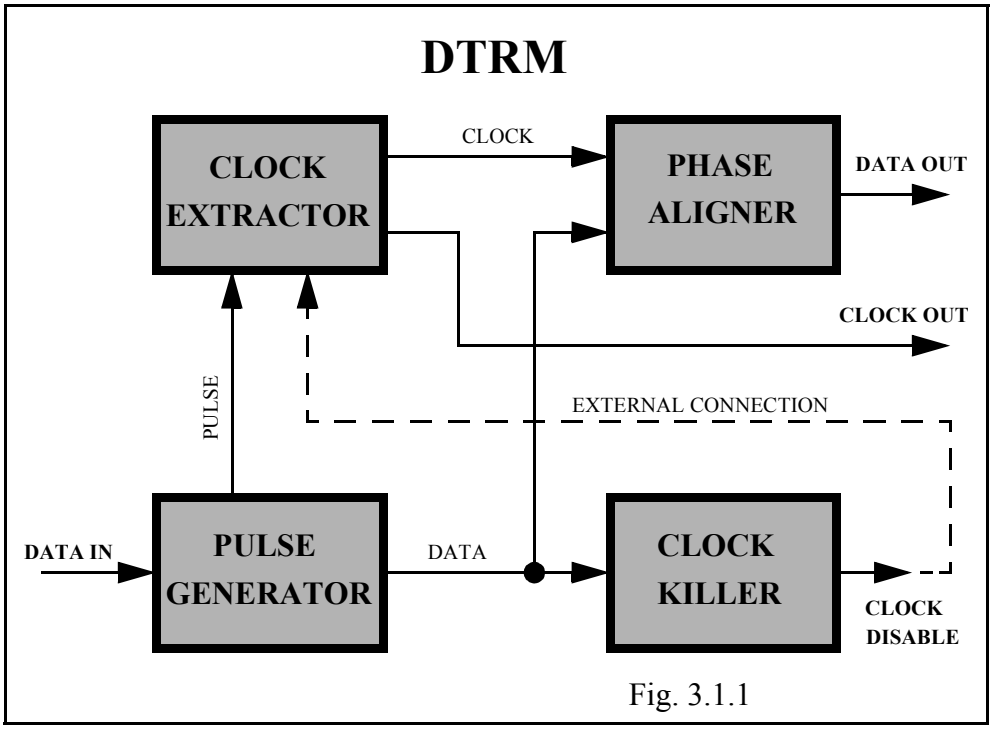

Fig. 3.1.1

The **PG** generates negative pulses of about 130 ps (~ 300 mVpp) during the data transitions. This stage contains also a buffer to distribute the data information to PA and CK circuits.

The **CE** stage extracts the timing information from data and it distributes the clock recovered to PA circuit and also to the output interface.
This stage can be disabled by the CK circuit, if necessary, by an external connection.

The **PA** stage provides to the data/clock phase alignment in order to have the positive clock edge in a correct position for the sampling.

The **CK** stage provides to cut off the output clock when there is no data at the input interface. This circuit can also be excluded for applications which don't need this feature.

The DTRM functionality is based on the PCO Clock Extractor which is the most important circuit. This peculiar application deserves more comments, so we think it is important to deepen this argument. The following chapters show some details about the PCO circuit in order to evaluate better its flexibility.

3.2 Analisys

The clock extraction problem isn't often easy to solve specially when the pattern used is poor of transitions. It is more difficult if we want to realize a simple clock recovery circuit too.
The SAW resonators alternative have too high Q value and we must decrease it for this application otherwise the maximum jitter tolerance will be too low to cover the requirements of commonly used protocols.

In the other hand, by using a LC resonator, special inductors and capacitor are needed in order to have a sufficient Q value to preserve the timing information during long "0" or "1" sequences. In this case the LC circuit is energized only by pulses generated during the data transitions.

The PCO clock extractor is an injection locking circuit realized only by an oscillator disturbed by pulses every data transition event.

In other words, the pulses generated every data transition synchronize the edge waveform produced by the oscillator.

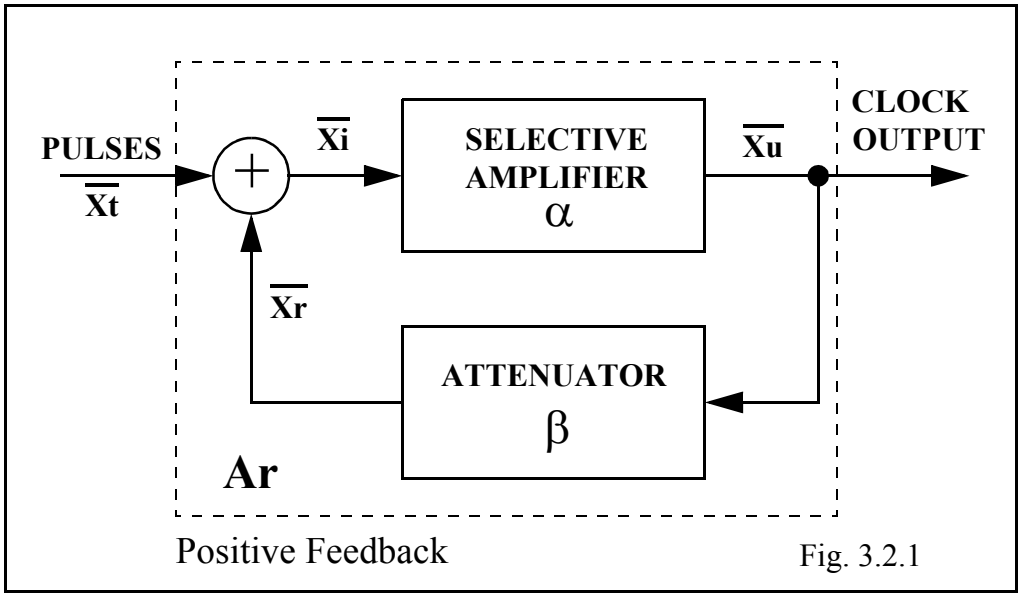

Fig. 3.2.1

The picture in fig. 3.2.1 shows the block diagram of PCO circuit. The transfer function of this architecture is in the following represented.

$$\bar{\alpha} = \frac{\overline{Xu}}{\overline{Xi}} \qquad \bar{\beta} = \frac{\overline{Xr}}{\overline{Xu}} \longrightarrow \qquad \overline{Xu} = \bar{\alpha}\overline{Xi} \quad \overline{Xr} = \bar{\beta}\overline{Xu}$$

$$\textit{but}\ \ \overline{Xt} = \overline{Xi} - \overline{Xr} \quad \textit{and} \quad \overline{Ar} = \frac{\overline{Xu}}{\overline{Xt}} \longrightarrow \overline{Ar} = \frac{\bar{\alpha}\overline{Xi}}{\overline{Xi} - \overline{Xr}}$$

$$\textit{so} \quad \overline{Ar} = \frac{\bar{\alpha}\overline{Xi}}{\overline{Xi} - \bar{\alpha}\bar{\beta}\overline{Xi}} = \frac{\bar{\alpha}}{1 - \bar{\alpha}\bar{\beta}} \quad (1) \qquad \begin{cases} \angle\bar{\alpha}\bar{\beta} = 0 \\ |\alpha\beta| \geq 1 \end{cases} \quad (2)$$

The condition (1) is applicable only if $|\alpha\beta| < 1$. In the other situations the poles analysis must be considered in the transfer function equations [1].
So, there are three possible conditions: $|\alpha\beta| < 1$, $|\alpha\beta| = 1$, $|\alpha\beta| > 1$.
The second one is also called Barkhausen condition and it represents the stability limit. Above this limit ($|\alpha\beta| > 1$) the Ar block starts to oscillate with an oscillation period that satisfy the condition (2).
Normally in the block diagram of an oscillator the $\overline{Xt}$ signal doesn't

appear because the oscillation can starts without it. The adder node doesn't appear too because $\overline{Xr}$ and $\overline{Xi}$ signals are the same parameter. But, in our application, we want to lock the oscillator with data timing, so we use the adder node to make a vectorial sum of the reaction vector with the synchronization signal ($\overline{Xt}$).
Moreover, the positive or negative edges of data, in the PCO circuit, is aligned with the negative clock edge in order to respect the setup and hold time for a correct data sampling.
In the oscillation condition the $\overline{Xr}$ signal is a cycling vector with the same phase of $\overline{Xu}$. If we inject another vector in the adder node, through the $\overline{Xt}$ input, we obtain the situation showed in fig. 3.2.2.

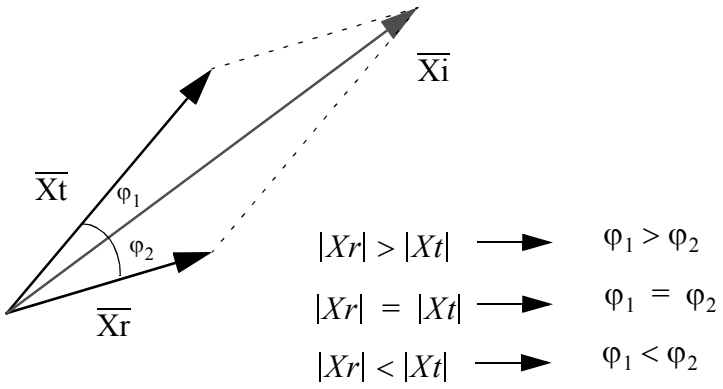

Fig. 3.2.2

The resultant vector ($\overline{Xi}$) depends on the amplitude and the phase parameters of the other two vectors $\overline{Xr}$ and $\overline{Xt}$.

3.3 Parameters

If $\overline{Xr} > \overline{Xt}$ the resultant vector is more affected by $\overline{Xr}$ parameters. It means also that the $\overline{Xt}$ vector doesn't produce relevant effects on $\overline{Xi}$, so it could cause only jitter at the oscillator output if the $\overline{Xt}$ frequency and the normal frequency of the oscillator are different.

If $\overline{Xr} = \overline{Xt}$, both of these components have the same effect on $\overline{Xi}$. In this condition the oscillator generates a signal not related to any of the two vectors. If $\overline{Xt}$ and $\overline{Xr}$ signals have the same frequency and, if the vectorial sum of them generate a resultant vector ($\overline{Xi}$) enough energized to stimulate the amplifier, the oscillation condition will be reestablished.

This is true also if the normal frequency of the oscillator and the frequency of $\overline{Xt}$ vector are similar but not the same, because the circuit is looped back then $\overline{Xr}$ parameters depends also from $\overline{Xt}$ (see the injection locked concept [2-4]). So, if $\overline{Xt}$ frequency is contained inside the amplifier bandwidth the resultant vector ($\overline{Xi}$) will follow the $\overline{Xt}$ one and the oscillation period will be controlled by the $\overline{Xt}$ frequency.

If $\overline{Xt}$ vector is switched off for a time of more than one period, the oscillator will be still active because the oscillation is guaranteed by $\overline{Xr}$. During this periods the phase difference between $\overline{Xr}$ and $\overline{Xt}$ (missing) will increase, but, when the $\overline{Xt}$ signal will be switched on again the $\overline{Xi}$ vector will be affected by a phase jump. The previous lock situation can be reestablished if this phase jump will be not so relevant to produce intermodulation products distributed out of the amplifier bandwidth (dependent from the Q of the output resonator). The same situation can be obtained also if $\overline{Xt}$ is an instantaneous vector (pulse) sometimes inserted in the adder node, but it must be bigger than the $\overline{Xr}$ vector ($\overline{Xt} > \overline{Xr}$ see fig. 3.2.2) in order to generate a relevant harmonic product contained into the amplifier bandwidth. In other word, we have made an injection locked circuit using a simple oscillator controlled by external pulses.

The limits of frequency for locking pulses depend from the amplitude of $\overline{Xt}$ and $\overline{Xr}$ vectors, from the frequency relation between them, and from the Q factor of the LC resonator implemented in the oscillator. The frequency relation between $\overline{Xr}$ and $\overline{Xt}$ vectors must be an integer number, and it could be time variable. The data transitions are time variable too, so they can synchronize the oscillator.
The pulses polarity is one of the most important parameter because it determines the clock edge polarity. In order to respect the data setup and hold time, we must use negative pulses.

In our application we have succeeded to extract the clock information from a serial data link (184.320 Mbit/s) which was composed by the following repetitive sequence: FFFFFFFFFFFF000000000000 (limit condition used only in the trimming phase).
So, we can guarantee the timing extraction from a pattern composed by the following repetitive sequence: FFFFFF000000 (24 bit at logic level "1" followed by 24 bit at logic level "0"). We have also tested this circuit with a pseudo random data pattern (2^{23}-1) without errors for 72 hours.

4 IMPLEMENTATION

4.1 Clock Extractor

We have used the PCO circuit previously described.
The oscillator is a grounded base Colpitts architecture implemented by a BFR92 transistor powered by a voltage regulator (3.6 V) to avoid frequency drift. The control pulses are directly injected in the emitter junction by a little decoupling capacitor.
The center frequency must be adjusted by using a data pattern which simulate the worst condition for the clock recovery operation. To do that, we have implemented a high performance variable inductor.
The oscillator output is buffered by an ECL line receiver which regulates automatically the clock duty cycle.

4.2 Pulse Generator

This circuit is implemented by an ECL differential splitter device. One of the two differential outputs is short circuited (OUT1 shorted with $\overline{\text{OUT1}}$). In this way, during a data transition, a pulse is generated on that node. The pulse characteristics depend on the reaction times of the ECL device.
The other output (OUT2) is used to drive the Phase Aligner circuit.

4.3 Phase Aligner

This function has to be done only by a ECL differential flip flop device which receives the data information from the line receiver input and the clock one coming from the PCO.

4.4 Clock killer

This circuit is implemented by a peak detector connected to a voltage comparator which has an open collector output stage. It switches off the PCO buffer when the data information is missing. The connection with the PCO buffer is external, so it can be removed if the PCO must be leaved in free running mode. In this case the PCO $\overline{\text{ENABLE}}$ pin must be connected to the negative power voltage.
This circuit can be used also as a loss of data alarm.

4.5 Interfaces

The data and clock I/O interfaces are differential ECL, if the power supply voltage is negative (with respect to the ground), and differential PECL if the power supply voltage is positive.
The input interface must be series terminated by a 100 ohm resistor and the output interfaces (data and clock) must be pull downed by 390 or 470 ohm resistors. In PECL mode the output interfaces must not be shorted directly to the ground otherwise the output drivers could be damaged.
The $\overline{\text{ENABLE}}$ clock is an open collector signal and it can be directly connected to the PCO $\overline{\text{ENABLE}}$ pin.

4.6 Mechanical description

The DTRM is an hybrid SIL circuit which have the following dimensions: (41,2 x 10,6 x 0.6 mm). A four layers impedance controlled PCB has been used and all components are distributed on the two external layers. An external metal shield has been used to prevent electro magnetic irradiations. This shield is virtually connected to the ground by using decoupling capacitors.

More information about UTRM physical structure will be given if requested.

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute maximum ratings

Table 1: Absolute maximum ratings (PECL mode)

Parameters	Min	Max
Supply voltage	-	+6.2 V
Input voltage	-0.4 V	+5.5 V
Output current	-	12 mA
Lead temperature	-	+285 C/10s
Storage temperature	-50 C	+120 C

5.2 Static characteristics

Table 2: Static characteristics (PECL mode)

Parameters	Min	Typ	Max
Supply voltage (Vcc)	+4.75 V	+5.0 V	+5.25 V
Supply current	150 mA	160 mA	175 mA
Power dissipation	710 mW	800 mW	920 mW
V_{OL}	-	Vcc - 1.7 V	-
V_{OH}	-	Vcc - 0.95 V	-
Input HIGH current	-	-	150 µA
Operating temperature	0 C	-	+50 C
Humidity	15%	-	90%

5.3 Dynamic characteristics

Table 3: Dynamic characteristics (UTRM-184)

Parameters	Min	Typ	Max
Bit rate	184.316 MHz	184.320 MHz	184.324 MHz
Clock duty cycle	45%	50%	55%
Jitter	-	0.03 UIpp	0.05 UIpp
Input swing	150 mV	800 mV	1400 mV
V_{CMR}	Vcc - 0.4 V	-	Vcc - 2.0 V
Raise/Fall time (output)	100 ps	225 ps	350 ps
Propagation data delay	3.20 ns	3.51 ns	3.82 ns
Cut off time	-	10µs	-

6 APPLICATIONS

6.1 USI4 Clock recovery

The UTRM has been designed for the USI4 interfaces to extract the timing information from serial data link at 184.320 MHz properly coded in order to have at least one data transition every 24 bits group.

6.2 STM1 Clock recovery

By using another value of variable inductor, the UTRM can be used also to extract the timing information from serial data link at 155.520 MHz (STM1) properly coded in order to have at least one data transition every 24 bits group.

6.3 Frequency multiplier

The UTRM can be used also as a frequency multiplier. For example, it can extract a 184.320 MHz signal frequency locked directly from a 2.048 MHz one. The multiplying factor must be an integer number (from 2 to 96).
By changing the variable inductor value it will be possible to extend the frequency operation limits from 150 MHz to 200 MHz with the same performances showed previously.

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