Title
Switch Element description

CONTENTS

1 INTRODUCTION

The SWitch Element (SWE) circuit is a basic building block,that was designed for the RACE1 Atmospheric demonstrator. The SWE circuit was used in the implementation of the SWitch Modules (SWM24 and SWM12). The SWE circuit is implemented as a full custom VLSI design using Texas Instrument 0.8u BiCMOS Technology. The circuit consists of two Switch Elements, each capable of handling one bidirectional serial link at 155.52 Mbit.

In the Switch Modules, the SWEs are connected in a ring structure. In the figure below, the SWE ring on the SWM12 board is illustrated.

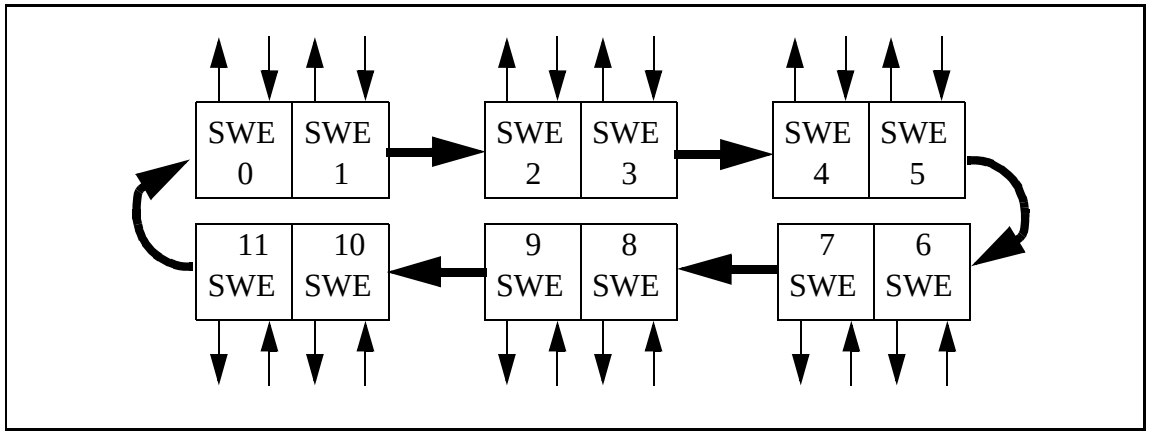

figure 1 SWM12.

The SWM12 ring consists of 6 SWE circuits, 3 circuits mounted on each side of the board. This solution gives a very short connection between two circuits. The SWM24 board is similar using 12 SWE circuits, 6 on each side. The cells received at the serial link of each SWE travels through the whole ring in one cell period.

The required cell format is a 5 bytes header, an extra byte (E) and a 48 bytes payload, see the figure below. The total cell length is 54 bytes

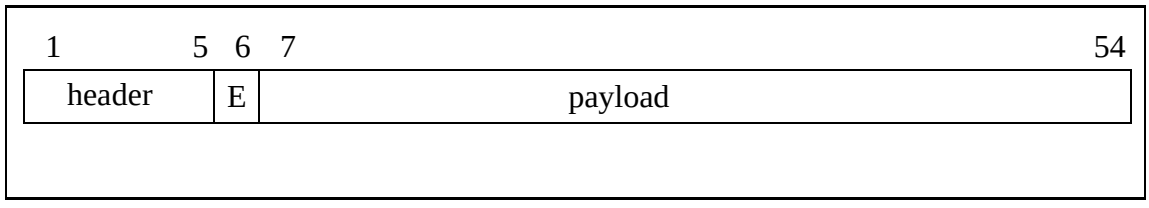

figure 2 The SWE cell format

In chapter 2 the common functions used by both Switch Elements in the SWE circuit are described. The Switch Element cell flow and clock handling functions are described in chapter 3. All SWE circuit signals are described in chapter 4. A simple programming model for the cell flow control and supervision is described in chapter 5. The SWE test mode is described in chapter 6. The electrical characteristics and mechanical data are described in chapters 7 and 8 respectively.

2 GENERAL CIRCUIT DESCRIPTION

An overall view of the SWE circuit is shown in the figure below. The SWE circuit can handle two bidirectional ATM cell streams at 155.52 Mbit.

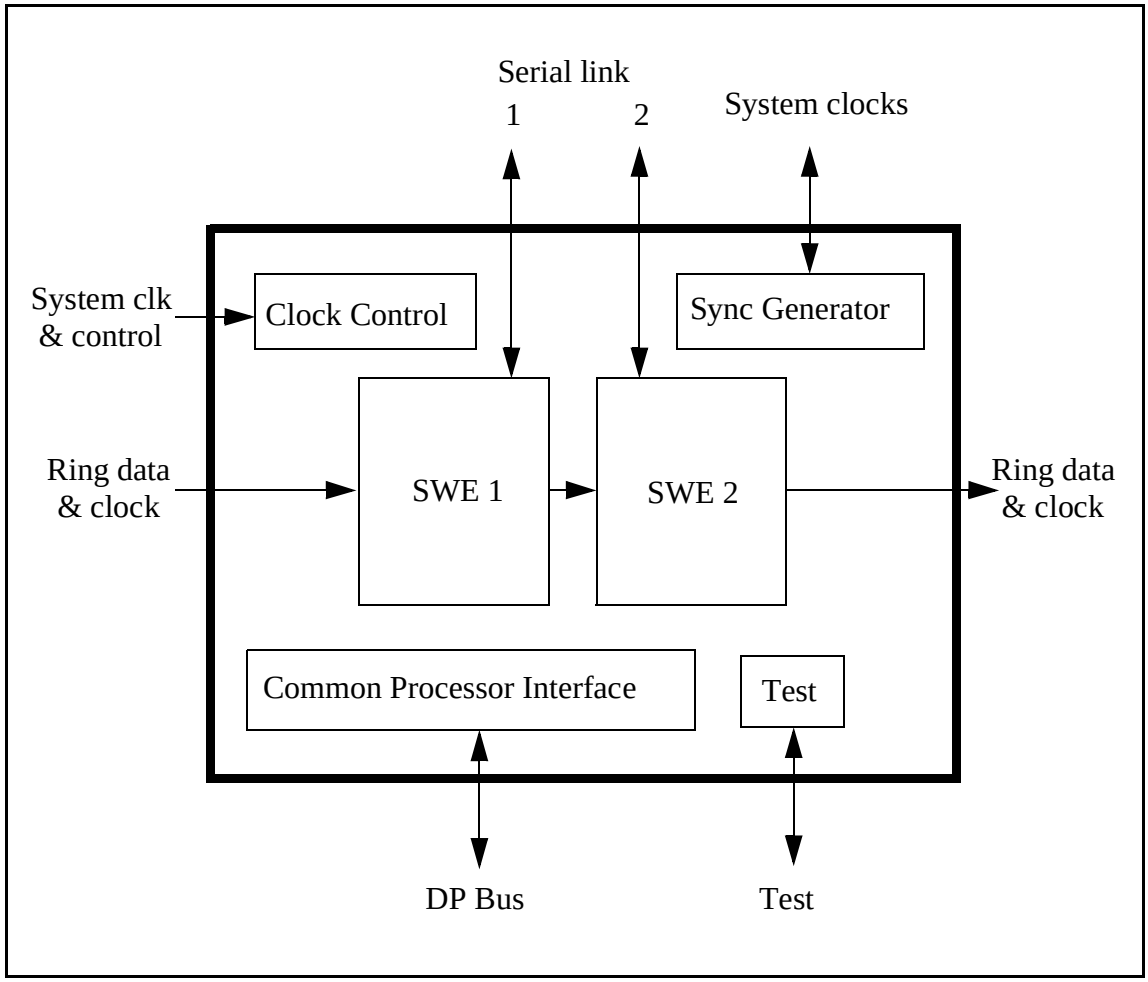

figure 3 The SWE circuit.

The circuit consists of two identical Switch Elements (SWE 1 and SWE 2) and a number of common functions. The Switch Element is described in the next chapter. Below follows a description of the common functions:

Sync Generator:

The Sync Generator creates a system sync signal (360 khz = cell frequency) and a system clock signal (155.52 Mhz). The signals are in phase. As master input clock, either an external 155.52 Mhz clock or one of the serial data clocks can be selected.

Clock Control:

The Clock Controller handles the system clocks distribution on the chip. It also controls the bit rate on the ring and the selection of the Sync Generator master clock input.

Common Processor Interface:

The Common Processor Interface handles the processor access to the selected SWE. The interface is designed to communicate with the Motorola 68000 processor family.

Test:

The test functions are used when testing mounted components. A number of internal nodes can be tested.

3 SWE DESCRIPTION

3.1 THE SWE CELLFLOW

The functions responsible of the cell flow through the Switch Element are shown in figure 4:

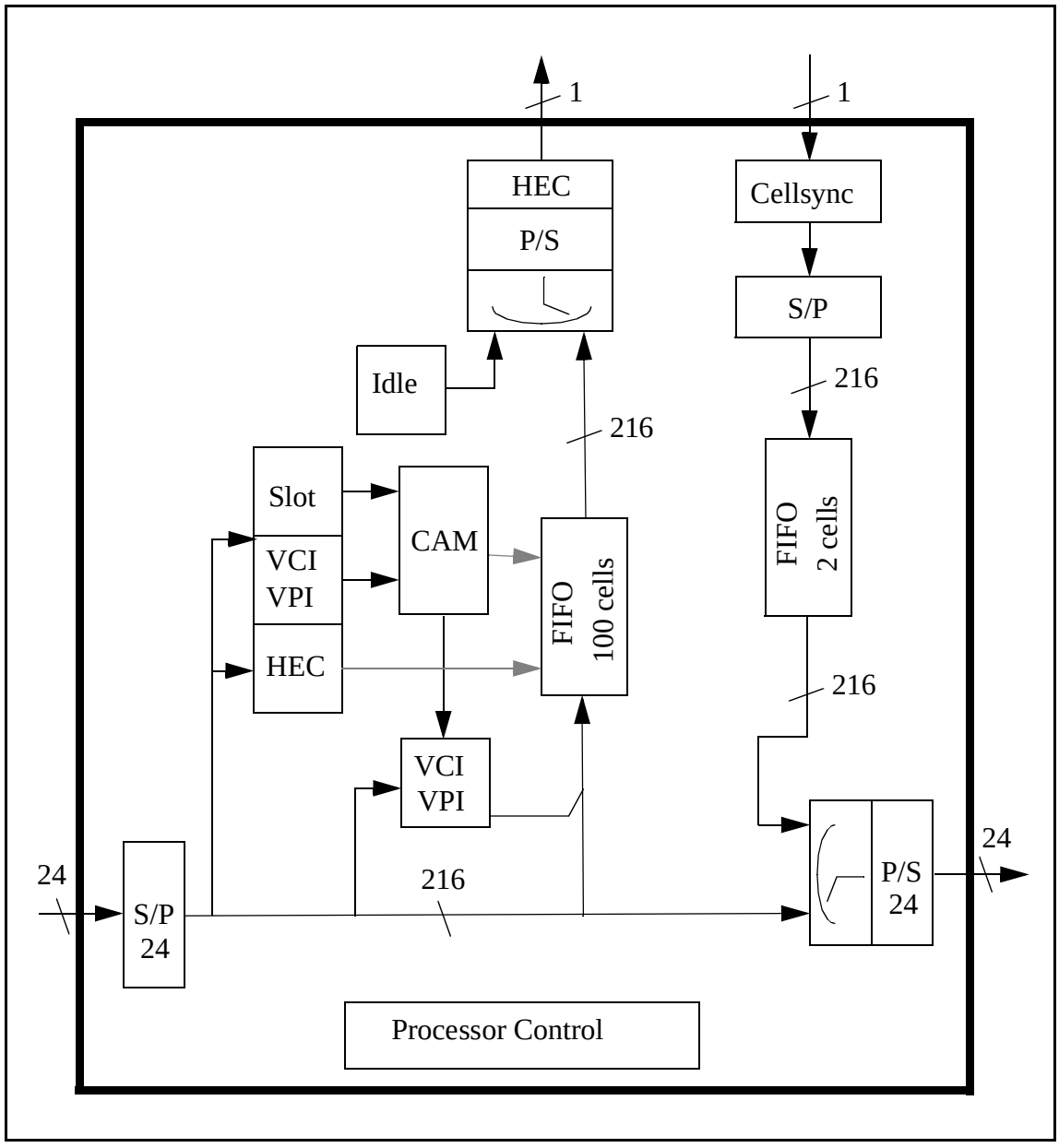

figure 4 The SWE circuit cell flow.

The received serial bit stream is synchronised and converted into parallel format. The received cells are passed through a buffer stage (small FIFO). The buffer stage is used to align the received cells with the cells on the ring.

The cell transfer around the ring (in one cell period) is divided into 24 or 12 (or 6 or 3, see clock handling) time slots. The selected number of time slots depends on the number of SWEs in the ring. The SWE transfers the received cell to the ring output during one time slot. The other time slots are used to transfer the cells from the ring input to the ring output.

At the ring input a slot counter is used to determine in which SWE the incoming cell is received. All cell headers received at the ring input are checked against a connection memory to see if the cell is to be switched to the link output or not. Also the HEC field is normally checked.

If the cell address (VPI or VCI) is defined in the connection memory and the HEC is correct, the cell is copied to a buffer stage (big FIFO). Remember that the cell also must be transferred to the ring output. The address field (VPI or VCI) of the copied cell will be changed to the value defined in the connection memory. If the received cell header is not defined in the memory or is erroneous, the cell is ignored and is only passed to the ring output.

Cells are read from the buffer stage and sent to the link output. If the buffer is empty, an idle cell is sent instead. The cells are serialized. A new CRC value is calculated and inserted in the HEC field.

Below follows a description of all functions responsible of the cell flow through the Switch Element:

Cellsync:

The Cellsync main function is to find the cell boundaries and maintain cell synchronisation of the incoming bitstream by means of checking the HEC field of each received cell. The cell stream is defined to be in sync when 7 or more consecutive cells with correct HEC is detected. Loss of sync is defined as 7 or more consecutive cells with HEC-error. The processor is informed about the sync-state by means of a status bit.

S/P Converter:

The serial cell stream is converted to a 216 bit (half cell) parallel format.

FIFO (2 cells):

The cell is temporarily loaded in a FIFO buffer while waiting to be read out to the ring. This FIFO is used to synchronize the serial link to the ring. The size of the FIFO is 2 whole cells. Cells are not loaded in this FIFO buffer if the link input is out of sync.

Ring Mux and P/S 24 Converter:

The ring multiplexer passes cells either from the FIFO buffer or the ring input. At time slot 0 the multiplexer selects the cell stored in the FIFO. In all other time slots the multiplexer selects the cell received at the ring input. The internal cell format of 216 bits is converted to 24 bits. During the current time slot, the whole cell is sent to the ring output as 18 words of 24 bit.

Ring S/P 24 Converter:

At the ring input the received cell 24-bit word format is converted to the internal 216-bit half cell format. The cell is forwarded to the switching logic and to the ring output.

HEC checker:

A CRC value is calculated on the first 4 bytes of the cell header. The CRC value is compared with the HEC field. The result is used in the decision whether the cell shall be switched or not.

VCI/VPI Selector:

The VCI/VPI Selector selects either VCI (12 bits) or VPI (12 bits) as the input address field to the connection memory. The selection is controlled by the processor.

Slot counter:

The Slot Counter keep a check on the current time slot. This counter value is used together with the VPI or VCI field of the received cell as data input to the connection memory. The counter value specifies from which SWE the cell is comming from.

CAM:

The connection memory is implemented as a CAM (Content Addressable Memory). It consists of 256 address positions. Each position has 17 data bits (5-bit time slot and 12-bit VPI/VCI).

Each received address field (VPI or VCI) together with the current time slot value is compared with the defined connections in the CAM. If a match is found a new 8-bit address value is valid at the CAM output. This value corresponds to the memory position where the match was found. If no match is found the output is not valid. The result is used in the decision whether the cell shall be switched or not.

All CAM positions can be written or read from the processor.

VCI/VPI Generator:

The VCI/VPI Generator changes either the VCI or VPI field in the cell header of the switched cells. Bits 7-0 of the selected field is loaded with the 8-bit value from the CAM. Bits 11-8 of the selected field are reset. The field that is not selected is not changed. The VCI or VPI selection is controlled by the processor.

FIFO (100 cells):

To allow short time bursts of switched cells, the SWE contains a FIFO capable of storing 100 cells. The FIFO also works as a synchronisation unit between the ring input and the link output.

If a match is found in the CAM and the HEC is correct, the cell is copied into the FIFO. The cell is stored in the FIFO until it is read out to the link output.

All FIFO positions can be read or written from the processor for test purposes. The FIFO has an overflow indicator and a cell counter that can be read by the processor.

Idle Generator:

The Idle Generator defines a 54 byte idle cell. If the FIFO is empty, the idle cell is passed to the link output.

Mux and P/S Converter:

The Link Multiplexer passes cells either from the FIFO buffer or the Idle Generator. The selected cells are converted to a 155.52 Mbit serial bitstream.

HEC Generator:

A new CRC byte is calculated on the first 4 bytes. This CRC byte is put in the HEC field.

Processor Control:

The Processor Control function directs writing and reading of the internal registers, which are used to control and supervise the cell flow. Also writing and reading of the memories (CAM and FIFO) is controlled by the Processor Control function.

3.2 CLOCK HANDLING

The SWE uses three different clock signals to control the cell flow

- Serial input data clock, 155.52 Mhz in phase with input data.

- System clocks consisting of a 155.52 Mhz clock and an in phase 360 khz sync clock (cell frequency).
- Ring input data clock and an in phase ring sync signal.

The serial input data clock and the system 155.52 Mhz clock must have exactly the same frequency to avoid cell loss at the ring output. Below follows a description on how each clock signal affect the cell flow.

3.2.1 Serial input Data Clock

The serial input Data Clock is used to control the data flow at the serial link receiver, see figure 5. All low frequency clocks and control signals at the link input is generated from this Data Clock. These low frequency signals are used to control the flow from the serial input to the buffer stage.

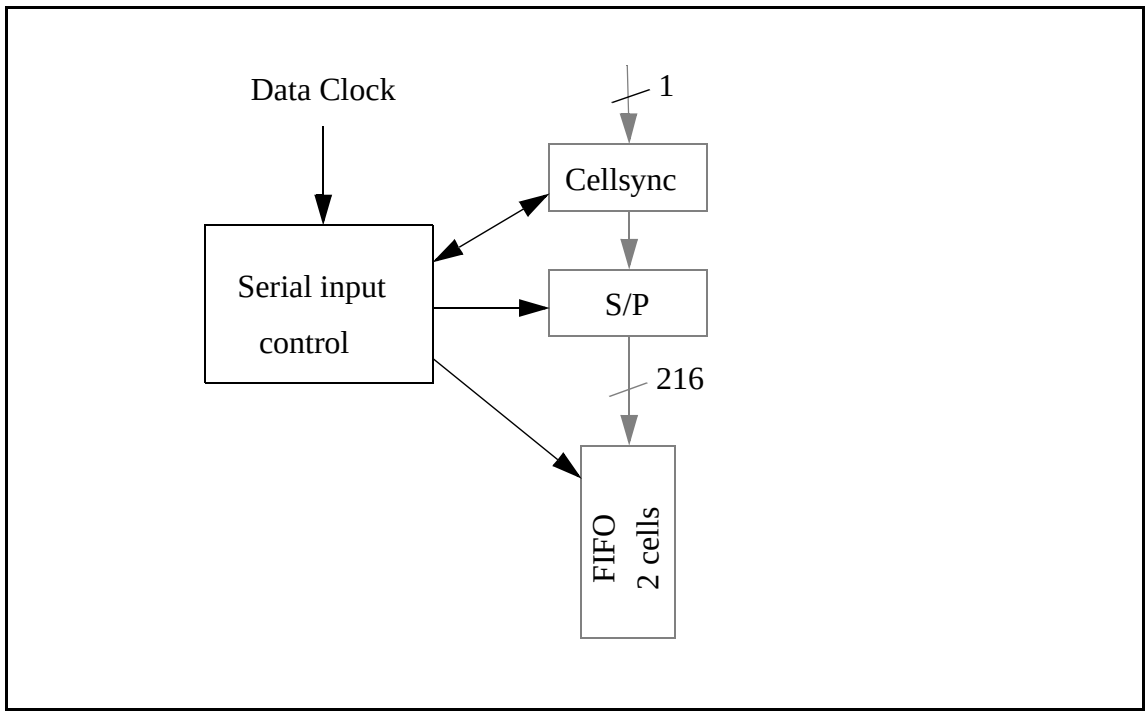

figure 5 The Serial Data Clock.

3.2.2 System Clocks

The System Clocks are used to control the cell flow at the serial link transmitter and at the ring output, see figure 6.

At the serial link transmitter, the clocks are used to generate all low frequency clocks and control signals that control the flow from the output buffer stage to the serial output. Also a data clock is created that is phase-aligned with the output data.

At the ring output, the system clocks are used to generate all low frequency clocks and control signals that control the cell flow from the input buffer stage to the ring output. Also a Ring Data Clock and Sync signal is created. These signals are phase aligned with the Ring Output Data.

The bit rate at the ring output is controlled externally by a **Clock Divider** function. A bit rate of 24*155.52, 24*155.52/2, 24*155.52/4 or 24*155.52/8 can be selected. The corresponding number of time slots are 24, 12, 6 or 3. The bit rate is selected by external signals and depends on the number of SWEs in the ring.

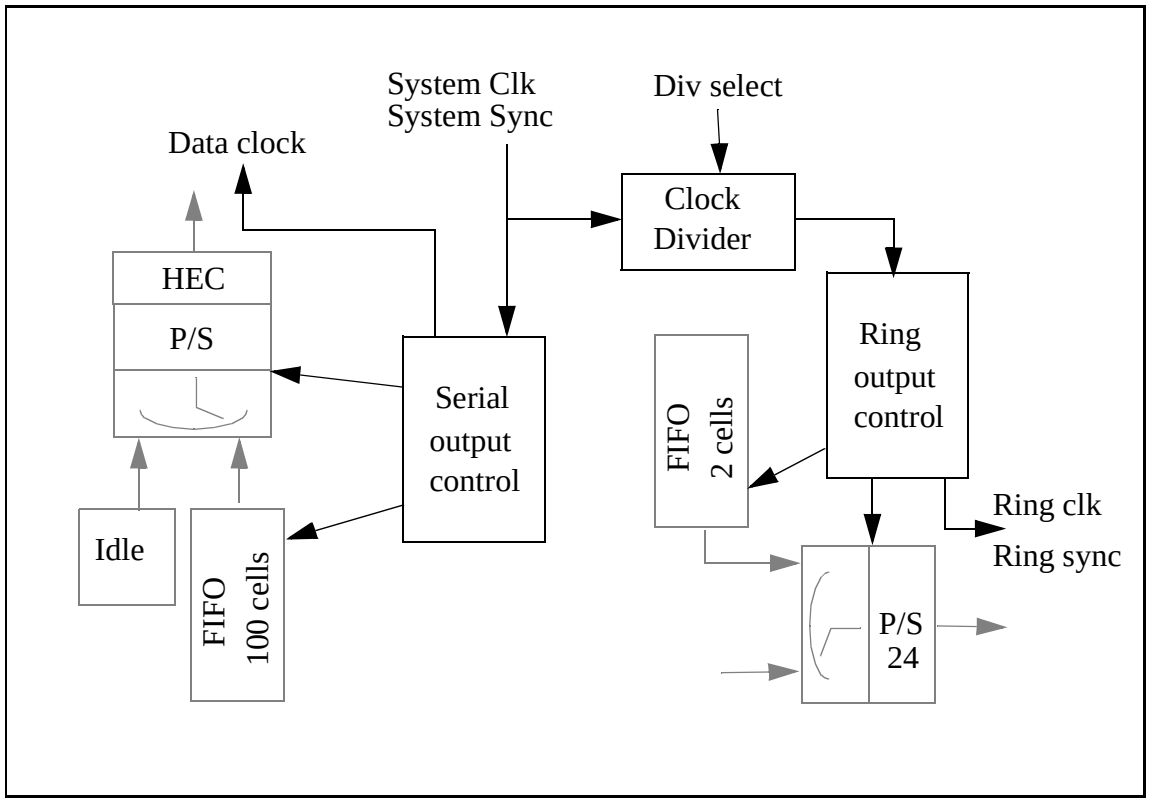

figure 6 The System Clocks.

3.2.3 Ring Input Clocks

The Ring Input Clock and Sync are used to control the cell flow at the ring receiver and the switching logic, see figure 7.

The clocks generates all low frequency clocks and control signals, that control the cell flow from the ring input to the ring output and from the internal ring bus to the output buffer stage.

The Ring Input Clocks also generates low frequency clocks, that are used in the Processor Interface for the synchronisation of the processor access.

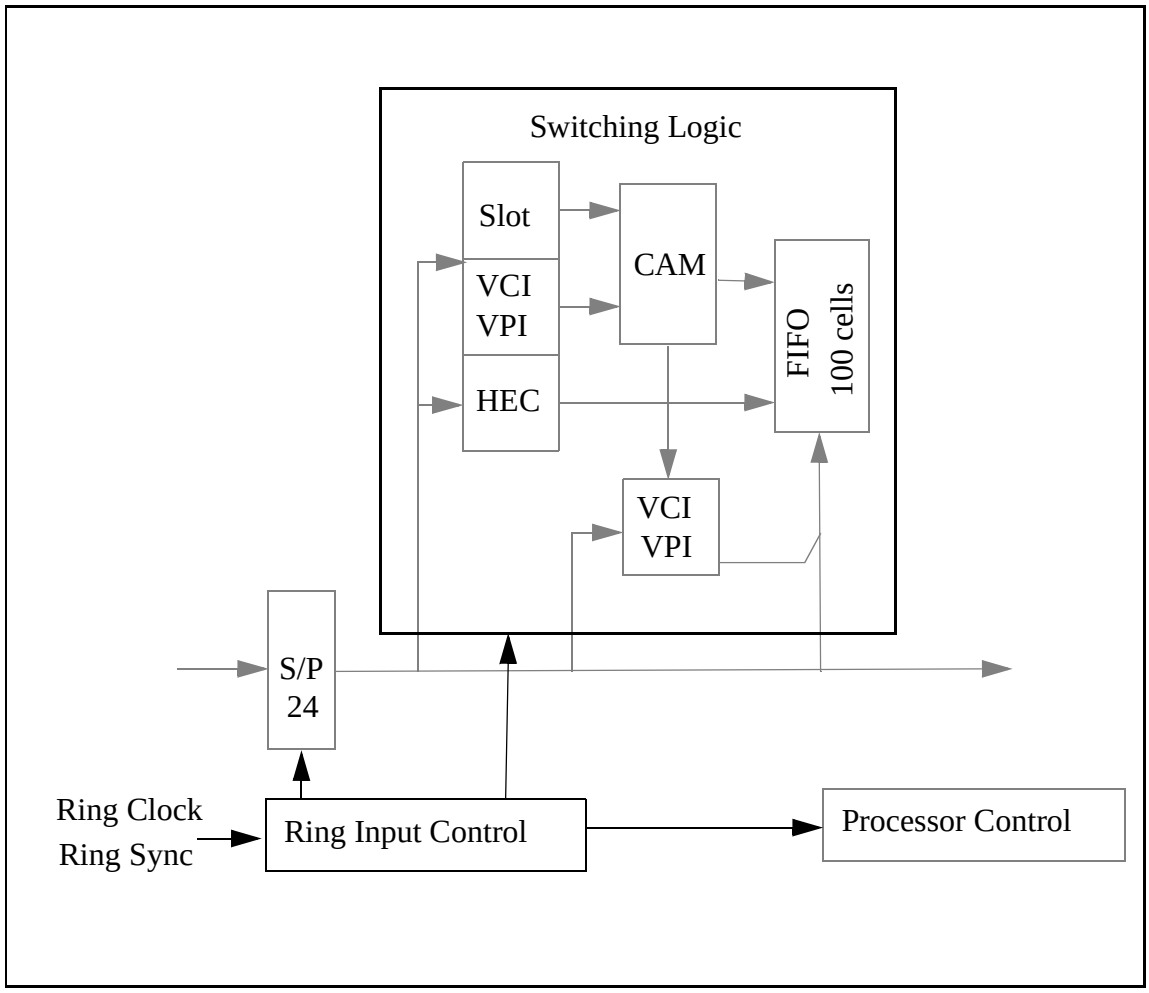

figure 7 The Ring Input Clocks.

4 SIGNAL DESCRIPTION

This section describes the SWE circuit pinout. The input and output signals are organized into the following functional groups (see figure 8):

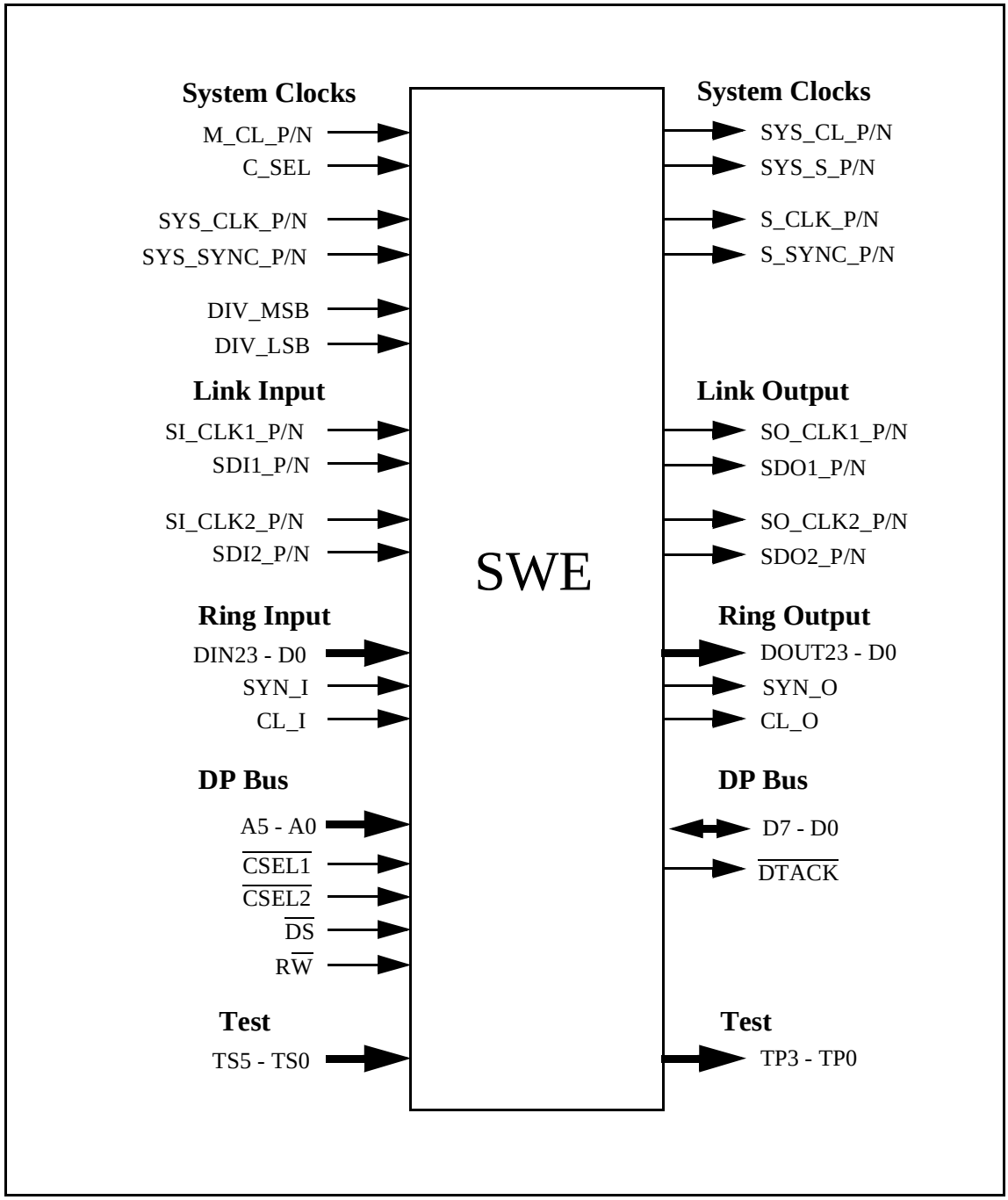

figure 8 Functional Signal Groups.

- System Clocks
- Link Input

- Link Output
- Ring Input
- Ring Output
- DP Bus
- Test

The circuit also has 33 power pins and 40 ground pins. Each signal group listed above is described below. P/N indicates differential (+ -) ECL signals.

4.1 SYSTEM CLOCKS

M_CL_P/N - Master Clock Input

This differential ECL input can be selected as input to the internal Sync Generator to generate the system clocks.

C_SEL - Clock Select input

This CMOS input is used to select either the M_CL input or the SI_CLK1 input as master clock to the internal Sync Generator.

SYS_CL_P/N - Master System Clock output

This differential ECL output is the 155.52 Mhz clock created in the Sync Generator. The clock is in phase with the SYS_S output.

SYS_S_P/N - Master System SYNC output

This differential ECL output is the 360 khz (cell frequency) clock created in the Sync Generator. The clock is in phase with the SYS_CL output.

SYS_CLK_P/N - System Clock input

This differential ECL input is the 155.52 Mhz clock needed for the Link and Ring transmitters. The clock must be phase aligned with the SYS_SYNC input.

SYS_SYNC_P/N - System SYNC input

This differential ECL input is the 360 khz (cell frequency) clock needed for the Link and Ring transmitters. The clock must be phase aligned with the SYS_CLK input.

S_CLK_P/N - System Clock output

Not used in Ring mode.

S_SYNC_P/N - System SYNC output

Not used in Ring mode.

DIV_MSB, DIV_LSB - Clock Divide select inputs

These CMOS input are used to select the bit rate at the ring output.

0,0 - 155.52 Mbit at each ring bit

0,1 - 155.52/2 Mbit

1,0 - 155.52/4 Mbit

1,1 - 155.52/8 Mbit

4.2 LINK INPUT

SI_CLK1_P/N - Serial Data Clock Input (SWE 1)

This differential ECL input is the 155.52 Mhz clock needed for the Link Receiver in SWE 1. The clock must be phase aligned with the SDI1 data input.

SDI1_P/N - Serial Data Input (SWE 1)

This differential ECL input is the Link Receiver data input to SWE 1. The data input must be phase aligned with the SI_CLK1 input.

SI_CLK2_P/N - Serial Data Clock Input (SWE 2)

This differential ECL input is the 155.52 Mhz clock needed for the Link Receiver in SWE 2. The clock must be phase aligned with the SDI2 data input.

SDI2_P/N - Serial Data Input (SWE 2)

This differential ECL input is the Link Receiver data input to SWE 2. The data input must be phase aligned with the SI_CLK2 input.

4.3 LINK OUTPUT

SO_CLK1_P/N - Serial Data Clock output (SWE 1)

This differential ECL output is the 155.52 Mhz clock created by the Link Transmitter in SWE 1. The clock is phase aligned with the SD01 data output.

SDO1_P/N - Serial Data output (SWE 1)

This differential ECL output is the Link Transmitter data output of SWE 1. The data output is phase aligned with the SO_CLK1 output.

SO_CLK2_P/N - Serial Data Clock output (SWE 2)

This differential ECL output is the 155.52 Mhz clock created by the Link Transmitter in SWE 2. The clock is phase aligned with the SD02 data output.

SDO2_P/N - Serial Data output (SWE 2)

This differential ECL output is the Link Transmitter data output of SWE 2. The data output is phase aligned with the SO_CLK2 output.

4.4 RING INPUT

DIN23 - DIN0 - Parallel Data Input Bus

This 24-bit CMOS bus is the Ring Receiver input. The data bus must be phase aligned both with the SY_I and CL_I inputs.

SY_I - Parallel Data Bus Sync Input

This CMOS signal is used to synchronise the cell flow at the Ring Receiver input. The signal is used to mark the beginning of the cell transfer at time slot 0. The signal must be phase aligned both with DIN23 - DIN0 and the CL_I inputs.

CL_I - Parallel Data Bus Clock Input

This CMOS signal is the data input clock needed for the Ring Receiver. The signal must be phase aligned both with DIN23 - DIN0 and the SY_I inputs.

4.5 RING OUTPUT

DOUT23 - DOUT0 - Parallel Data Output Bus

This 24-bit CMOS bus is the Ring Transmitter data output. The data bus is phase aligned both with the SY_O and CL_O outputs.

SY_O - Parallel Data Bus Sync Output

This CMOS output signal is the Ring Transmitter 360 khz (cell frequency) sync output. The signal marks the beginning of the cell transfer at time slot 0. The signal is phase aligned both with DOUT23 - DOUT0 and the CL_O outputs.

CL_O - Parallel Data Bus Clock Output

This CMOS output signal is the data clock created by the Ring Transmitter. The signal is phase aligned both with DOUT23 - DOUT0 and the SY_O outputs.

4.6 DP BUS

A5 - A0 - Address Bus input

This TTL input bus is used to address the internal registers and memory buffers during a read/write operation.

D7 - D0 - Data Bus input/output

This bidirectional three-state TTL bus is used to transfer data during a read/write operation.

$\overline{\textbf{CSEL1}}$ - Chip Select input (SWE 1)

This TTL input is used to address SWE 1. When the signal is at a low level, it enables read or write operations to internal registers and memories in SWE 1.

$\overline{\textbf{CSEL2}}$ - Chip Select input (SWE 2)

This TTL input is used to address SWE 2. When the signal is at a low level, it enables read or write operations to internal registers and memories in SWE 2.

$\overline{\textbf{DS}}$ - Data Strobe input

This TTL input is used to enable the data transfer at the data bus. The signal is active low.

R$\overline{\textbf{W}}$ - Read/Write input

This TTL input is used to control the direction of data flow. The signal is high for a read operation and low for a write operation.

$\overline{\textbf{DTACK}}$ - Data Transfer Acknowledge output

This three-state TTL output is used to indicate the completion of a read/write operation to the DP. The signal is active low.

4.8 TEST

TS5 - TS0 - Test Select inputs

These CMOS inputs are used to address different internal nodes which are multiplexed to the TP3 - TP0 outputs. These signals are only used when testing the chip.

TP3 - TP0 - Test outputs

These CMOS outputs show the signal levels at the internal nodes selected by the TS5 - TS0 inputs. These signals are only used when testing the chip.

5 PROGRAMMING MODEL

In this section, the different registers used for the control and supervision of the cell flow in each SWE are described. The internal addresses and instruction codes are the same for both SWEs. Selection of SWE is made externally (CSEL1 and CSEL2 signals). The SWE can work in normal mode or test mode. Only the normal mode is described in this chapter. Registers used for test purposes are described in the next chapter. The writeable registers used for the cell flow control and the readable registers used for the cell flow supervision are described separately. The address map of the registers is shown in figure 9.

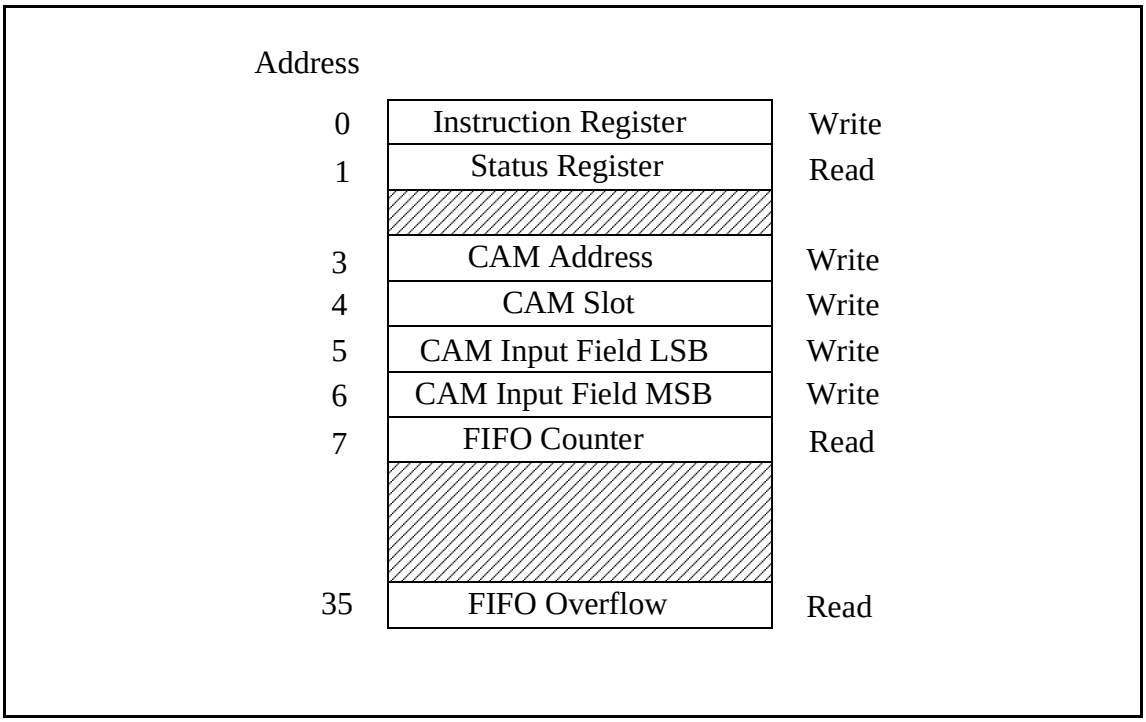

figure 9 The internal register address map, normal mode.

5.1 WRITEABLE REGISTERS

Two sets of writeable registers are used to control the cell flow in the SWE. The **Instruction Register** is used to set the SWE working mode and to execute a connection memory command. A set of **connection memory registers** are used to define a new connection or to erase an old connection.

5.1.1 Instruction Register (Address = 0)

This one byte register is used at restart to setup the working mode of the SWE. It also is used in run time to setup and release connections. Each instruction is defined by a unique value at the data bus (D7 - D0) input. The following instructions are used in normal operation:

RESET (D7-D0 = 01 hex):

SWE Reset command. Used at restart to set the SWE at a predefined state. The output FIFO buffer is emptied. The FIFO overflow indicator and FIFO counter are reset. The VCI field is selected both as input to and output from the connection memory. The HEC checker function is enabled and the HEC-error indicator is reset.

RESET STATUS (D7-D0 = 03 hex):

SWE Reset Status command. Used in run time to reset the HEC-error indicator and the FIFO overflow indicator.

WRITE CAM (D7-D0 = 0B hex):

Execute connection memory write command. Used to setup or release a predefined connection.

SELECT VCI (D7-D0 = 11 hex):

Select VCI field command. Used to select the VCI field as the input address to the connection memory (default).

SELECT VPI (D7-D0 = 13 hex):

Select VPI field command. Used at restart to select the VPI field as the input address to the connection memory.

GENERATE VCI (D7-D0 = 1D hex):

Generate VCI field command (default). Used to select the VCI field as the output address from the connection memory. The VCI field (bit 7-0) of the switched cells are changed by the 8-bit value from the connection memory. The next 4 high order bits (11-8) are reset. The 4 most significant bits (15-12) are not changed. The VPI field is not changed.

GENERATE VPI (D7-D0 = 1F hex):

Generate VPI field command. Used at restart to select the VPI field as the output address from the connection memory. The VPI field (bit 7-0) of the switched cells are changed by the 8-bit value from the connection memory. The 4 most significant bits (11 - 8) are reset. The VCI field is not changed.

SELECT HEC CHECK (D7-D0 = 19 hex):

Select HEC error check command (default). Used to enable the HEC checker function at the ring input. Only cells with correct HEC field are switched and loaded into the output FIFO buffer.

SELECT HEC BYPASS (D7-D0 = 1B hex):

Select HEC-error bypass command. Used to disable the HEC checker function at the ring input. Both cells with correct and incorrect HEC field are switched and loaded into the output FIFO buffer.

5.1.2 Connection Memory Registers

This 4 byte register set is used to define the input and output addresses of the connection memory at connection setup and release. The following registers are used in normal operation:

CAM Address Register (Address = 3)

This register is used to store the output value that will be loaded in the VPI or VCI field of the switched cells. The output value corresponds to the memory position. The same address must be loaded when the connection is released.

CAM Slot Register (Address = 4)

This register is used to store the time slot for the cell to be switched. The time slot value corresponds to a specific SWE number. In a 24 SWE Switch Module the values 0-23 should be used while in a 12 SWE Switch Module the values 0-11 should be used. When the connection is released, this register must be loaded with 1F hex.

CAM Input Field LSB Register (Address = 6)

This register is used to store the 8 least significant bits of the VPI/VCI field for the cells to be switched. When the connection is released, this register must be loaded with FF hex.

CAM Input Field MSB Register (Address = 5)

This register is used to store the 4 most significant bits of the VPI/VCI field for the cells to be switched. When the connection is released, this register must be loaded with 0F hex.

The connection memory is not erased at power up or reset. The software is responsible to erase the whole connection memory at restart. This is done by writing the FREE MEMORY DATA (slot = 1F hex, CAM input field lsb = FF hex, CAM input field msb = 0F hex) at all CAM positions.

The software is also responsible of not writing the same connection data at more than one CAM position. Each CAM position must contain unique connection data.

5.2 READABLE REGISTERS

Three readable registers are used to supervise the cell flow in the SWE. The **Status Register** shows the working mode and if errors have been detected at the Link and Ring receivers. The **FIFO counter** shows the current number of cells stored in the output FIFO buffer. The **Fifo Overflow Register** shows if the output FIFO has been overflowed, i.e. cell loss has occurred.

5.2.1 Status Register (Address = 1)

The status register is an 8-bit register showing the current working mode and detected errors. Each data bit (D7 - D0) is described below:

D(0): SWE MODE

0: Normal (traffic) mode (default)

1: Test mode

D(1): VCI/VPI SELECT

0: VCI input address selected (default)

1: VPI input address selected

D(2): VCI/VPI GENERATE

0: VCI field is changed (default)

1: VPI field is changed

D(3): HEC CHECKER SELECT

0: HEC Checker enabled (default)

1: HEC Checker disabled

D(4): HEC ERROR INDICATOR

0: No HEC-error detected at Ring input

1: HEC-error detected at Ring input

D(5): Not used

D(6): Not used

D(7): LINK INPUT SYNC INDICATOR

0: Link input out of sync

1: Link input in sync

5.2.2 FIFO Counter (Address = 7)

The 8-bit FIFO Counter shows the current number of half cells stored in the output FIFO buffer. As the buffer size is 100 cells the value range is 0 - 200. The counter is reset and the FIFO is emptied by a RESET command.

5.2.3 FIFO Overflow Register (Address = 35)

The FIFO Overflow Register indicate if overflow has occurred in the output FIFO buffer since the last RESET or RESET STATUS command. Only bit D(0) is relevant.

D(0) = 0: No cell loss in FIFO

D(0) = 1: Cell loss detected

6 SWE TEST MODE

In this section, a guideline on how to test the SWE circuit is given. First the different registers used for test purposes are described. Then the use of these registers to test the CAM and FIFO is described. To test the SWE circuit completely, a lot of software is needed.

6.1 SWE REGISTERS

As mentioned before, The SWE can work in normal (default) or test mode. In figure 9, the address map for the normal mode was shown. All these registers are used in test mode as well. There is a number of registers that are only used in test mode. The address map of these registers is shown in figure 10. The internal addresses and instruction codes are the same for both SWEs. Selection of SWE is made externally (CSEL1 and CSEL2 signals).

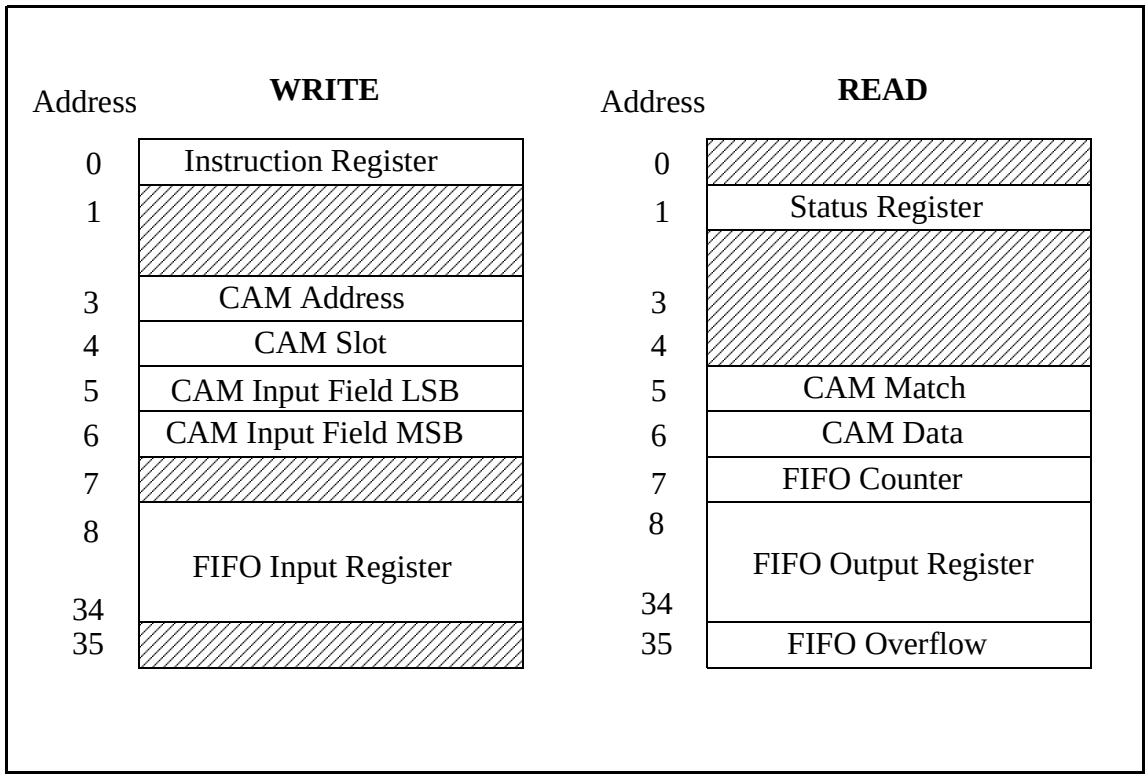

figure 10 Test registers address map.

6.1.1 Test Instructions

Some additional instructions are included in the test mode. These are written to the **Instruction Register** (Address = 0).

WRITE FIFO (D7-D0 = 05 hex):

Execute FIFO buffer write command. The data defined in the **FIFO input register** is written to the next free position in the FIFO buffer.

READ FIFO (D7-D0 = 07 hex):

Execute FIFO buffer read command. The data stored in the next read position in the FIFO buffer is written to the **FIFO output register**. If the FIFO is empty, no data is written.

READ CAM (D7-D0 = 09 hex):

Execute connection memory read command. The data in the **CAM Slot**, **CAM Input Field LSB** and **CAM Input Field MSB** registers are compared with the content at all CAM positions. The result is stored in the **CAM Data** and **CAM Match** registers.

SET NORMAL MODE (D7-D0 = 0D hex):

Set the SWE in normal mode command.

SET TEST MODE (D7-D0 = 0F hex):

Set the SWE in test mode command.

6.1.2 Connection Memory Registers

The following registers contain the result of the latest **READ CAM** command:

CAM Match Register (Address = 3)

This register indicates if a match has been found in the CAM. Only bit D(0) is relevant.

D(0) = 0: No match in CAM

D(0) = 1: Match found in CAM

CAM Data Register (Address = 4)

This register indicates the memory position where the match was found. If no match was found, the data is equal to zero. If match was found in more than one position, the data is not valid. Each CAM position must contain unique connection data.

6.1.2 FIFO Registers

There are two registers for the processor access to the FIFO. The processor can not access the FIFO buffer directly. Instead the processor writes or reads data to/from the FIFO registers. The transfer of data between these registers and the FIFO buffer is performed by the **READ FIFO** or **WRITE FIFO** commands.

FIFO Input Register (Address = 8 - 34)

This 27-byte register is used for loading a half cell. This half cell is then transferred to the FIFO buffer by the **WRITE FIFO** command.

FIFO Output Register (Address = 8 - 34)

This 27-byte register contains the current half cell after a **READ FIFO** command. The processor can then read the half cell directly from this register.

6.2 SWE TESTING

The CAM and FIFO are tested by using the registers described above. First the data is written to the input registers. Then the **WRITE** command is executed. This procedure is repeated for each memory position.

To check the CAM content the data must first be written to the input registers again. Then the **READ CAM** command is executed. The output registers are finally read by the processor. This is repeated for each position.

To check the FIFO buffer, first the FIFO Counter and the Overflow indicator are checked. Then the **READ FIFO** command is executed. The current half cell can now be read from the FIFO output register. This is repeated until the FIFO is empty.

The SWE can be used as a cell generator. Up to 100 different cells can be loaded in the FIFO buffer from the processor. By executing the **SET NORMAL MODE** command, all cells will be transferred to the link output. In this way, a one shot cell stream is created.

A continuous cell stream can be created in a ring structure. If the link output is looped to the link input, the cells will be received at the ring input. If the cell addresses are setup in the CAM, the cells will be loaded in the FIFO again.

The SWE can also be used as a cell recorder. All cells received at a desired link input can be switched to the FIFO buffer, if the corresponding cell addresses are setup in the CAM. The FIFO can be filled (100 cells) if an extra connection is setup. For instance, this extra connection can be an idle cell from another time slot (higher number). This ensures that the FIFO will be loaded with more than one cell per cell period. Thus the FIFO will be filled. When filled, the FIFO will only be loaded with cells belonging to the lowest time slot number. The other cells will be discarded, because the FIFO is overflowed.

When filled, the FIFO can be "stopped" by executing the **SET TEST MODE** command. The FIFO content can then be read by the processor.

A combination of the cell generator and recorder facilities can be used to detect cell bit errors and to measure cell delays. A lot of software handling cell generation and recording was developed for the RACE1 Atmospheric demonstrator.

7 ELECTRICAL CHARACTERISTICS

The SWE circuit has 40 ground pins and 33 power pins. The supply voltage for 25 of these power pins must be 5V. 8 power pins are used separately for the Ring Output. The supply voltage for these pins can be 3 - 5V. The lower voltage is used to reduce the power consumption.

The power consumption has been measured to be about 2 W. This value was measured with maximum bit rate and a supply voltage of 3 V at the ring output.

The ring outputs are designed to handle the cell transfer to the next ring input at maximum bit rate. The distance should not be longer than 2 cm. At lower bit rates the distance can be longer.

All ECL signals are differential (P/N) with pseudo ECL levels. The ECL input levels are in accordance with commercial ECL circuit levels. The ECL output levels are lower than in commercial ECL circuits. The voltage swing of each ECL output, loaded with a 60 ohm resistor, has been measured to be at least 200 mV peak to peak. i.e. the differential voltage swing is +- 200 mV.

All DP signals have TTL-levels in accordance to commercial LS TTL circuits. The capacitance of all inputs is about 5 pF.

Figure 11 shows how the ECL signals are connected between the SWE circuit and a commercial ECL circuit, located on another board. It is important that the power supplies are floating relative each other to avoid short circuits.

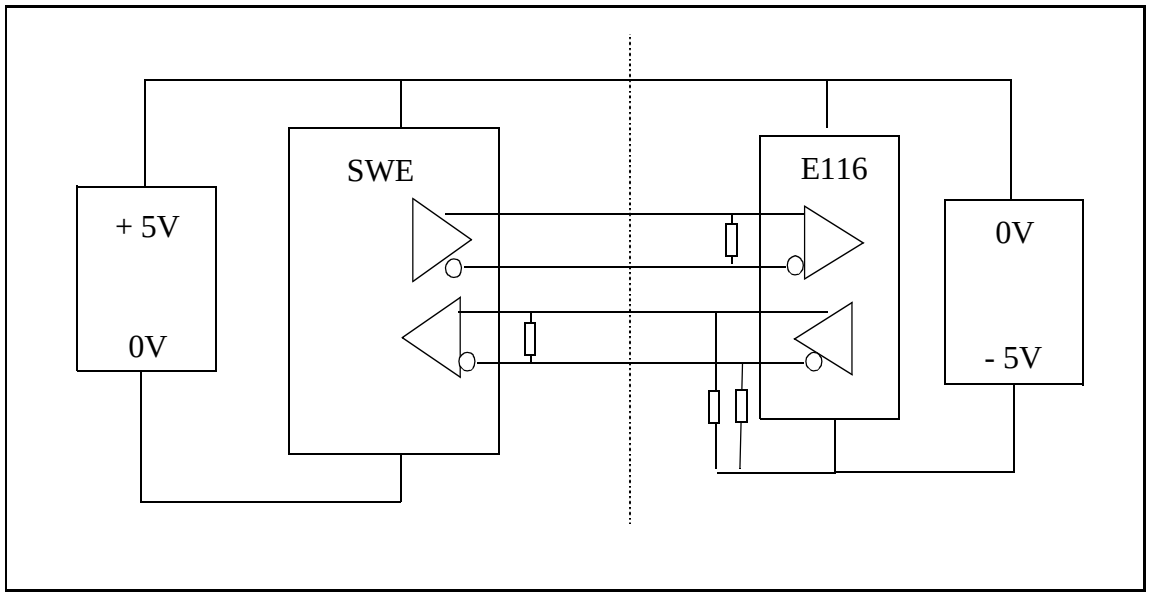

figure 11 Connecting the ECL signals.

TIMING DIAGRAMS

Input and output timing diagrams are shown below. The duty cycle of input clocks are assumed to be 50%. The duty cycle of all output clocks have been measured to be within 48 - 52 %. The difference between P and N of the ECL signals has been measured to be < 0,1 ns. Only the P signals are shown in the figures.

SYSTEM CLOCKS

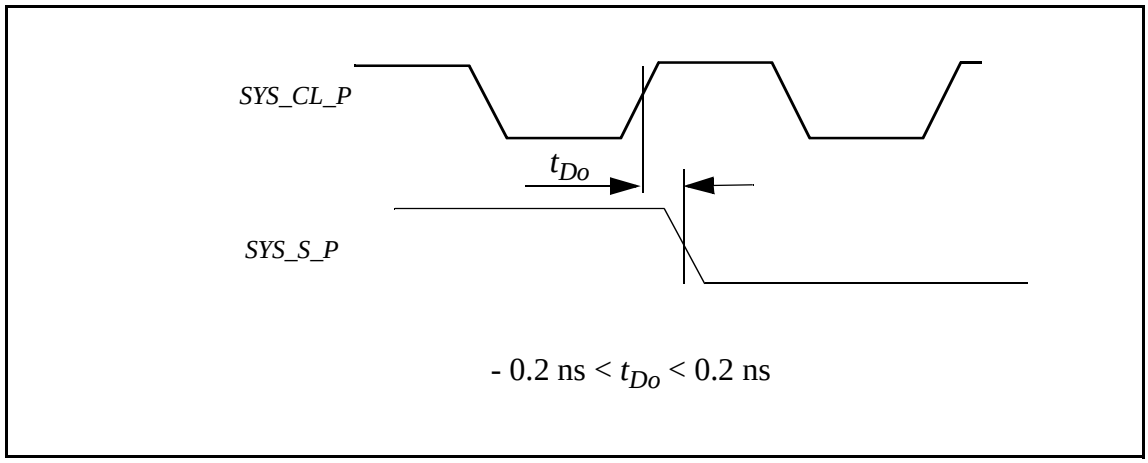

figure 12 Sync Generator output.

SYS_S is changed on the positive transition of the SYS_CL clock.

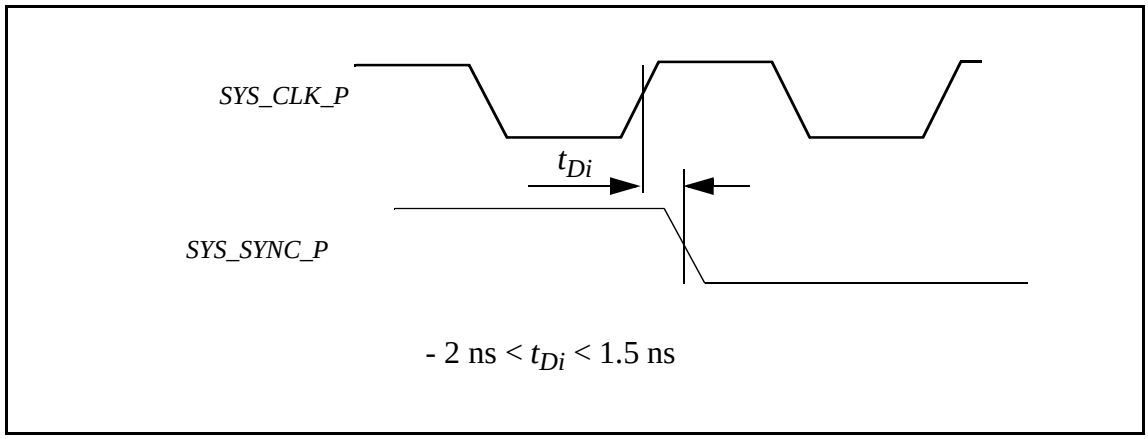

figure 13 System Clock input.

SYS_SYNC is internally clocked on the negative edge of the SYS_CLK clock.

As can be seen from the figures above, the Sync Generator outputs can be connected to the System Clock inputs. No termination is needed because of the short distance between the pins, see chapter 8.

LINK INPUT AND OUTPUT

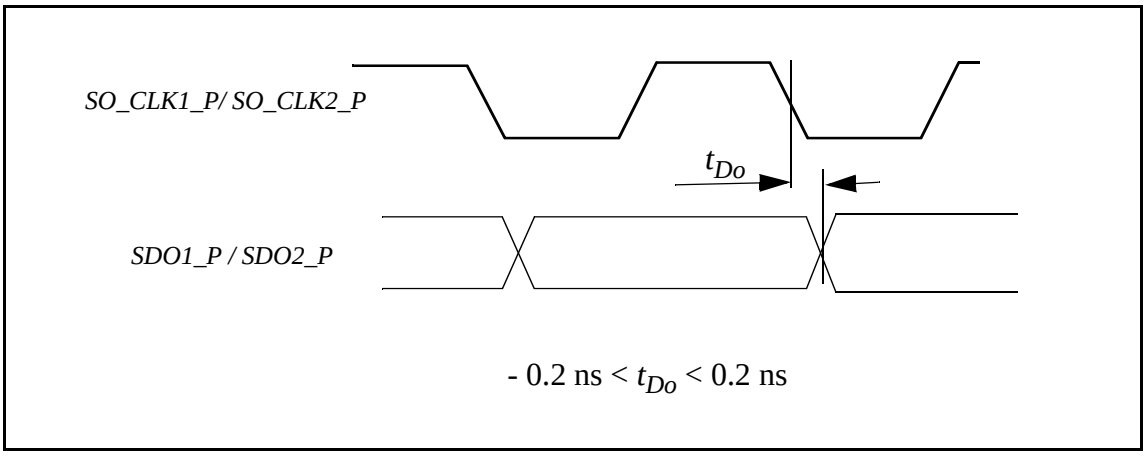

figure 14 Link output.

The serial data is changed on the negative transition of the output clock.

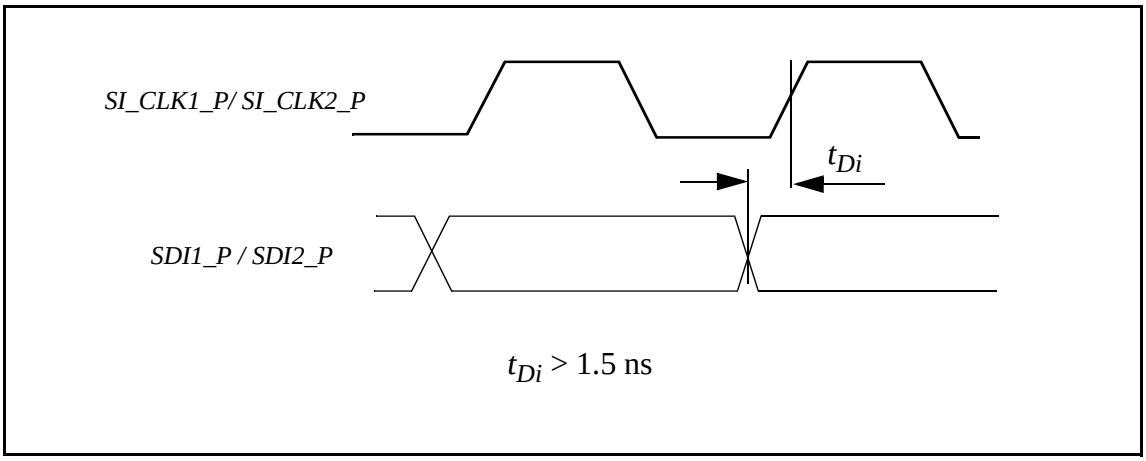

figure 15 Link input.

The serial data is internally clocked on the positive edge of the input clock. Two SWEs can easily transfer serial cell streams between each other. As can be seen from the figures above, the data is allowed to drift away up to 1,5 ns relative to the clock.

RING INPUT AND OUTPUT

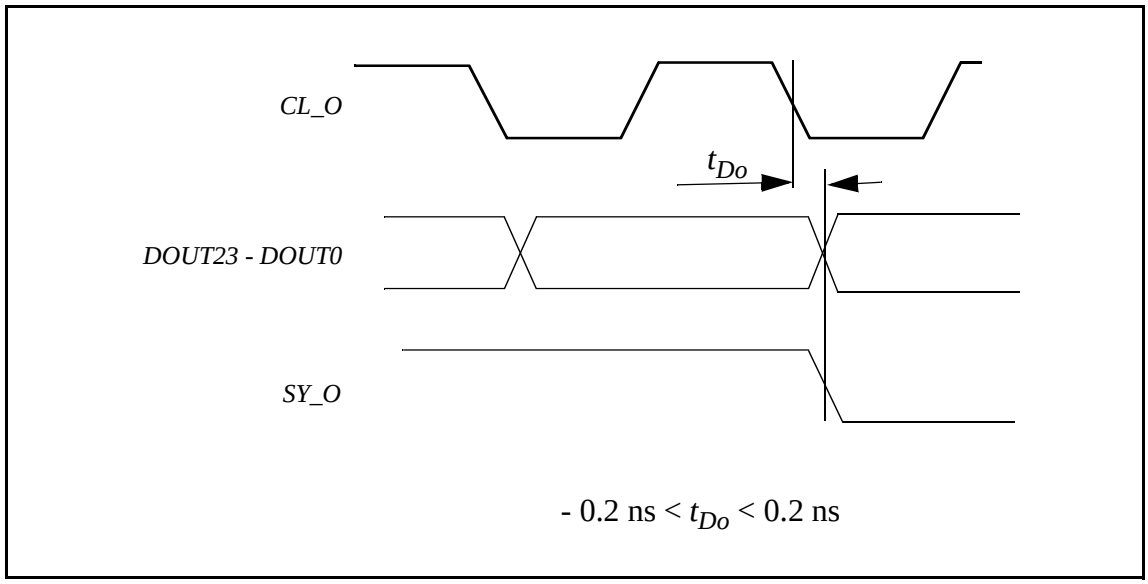

figure 16 Ring output.

Both the data and SY_O are changed on the negative edge of CL_O.

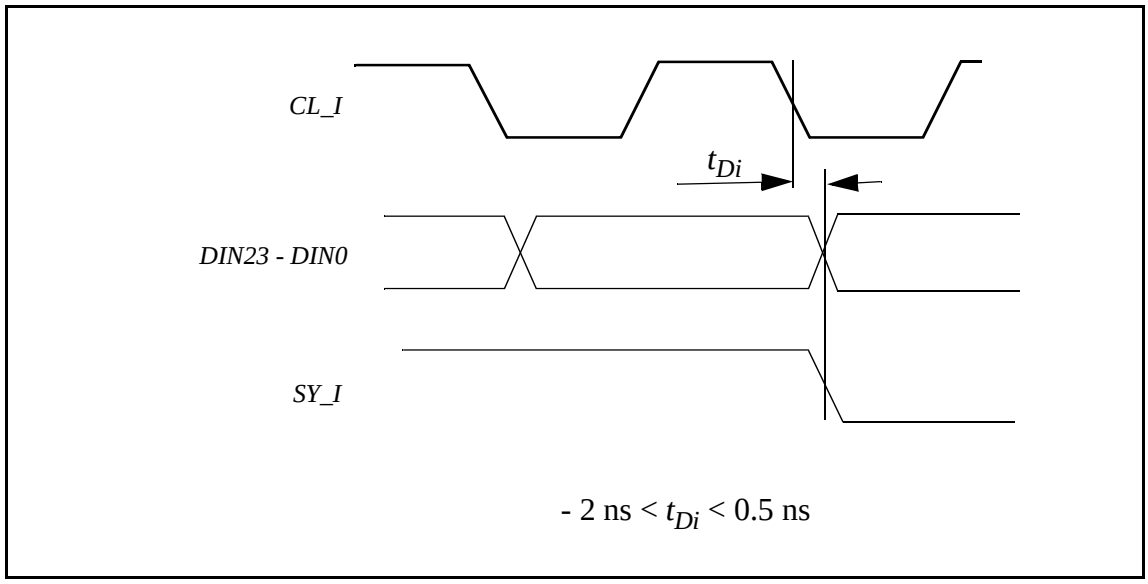

figure 17 Ring input.

The data is internally clocked on the negative edge (delayed) of CL_I, while SY_I is clocked on the positive edge of CL_I.

As can be seen from the figures above, the ring outputs can be connected directly to the ring inputs.

DP ACCESS

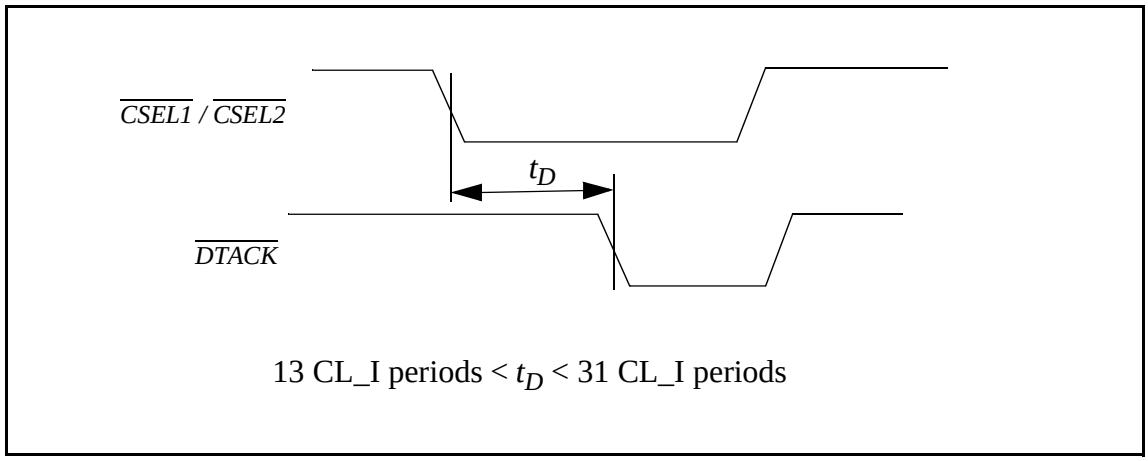

figure 18 DP access.

The DP interface is designed to communicate with a Motorola 68000 processor. See the 68000 Manual for more details about the processor access.

8 MECHANICAL DATA

The SWE chip is mounted in a TAB package. The component is mounted "die face down", i.e. the active chip-side is faced to the PCB ("flip-TAB"). The dimensions of the chip is 10 x 10 mm and the dimensions of a mounted TAB package is 19 x 19 mm. A mounted TAB package is shown in figure 19.

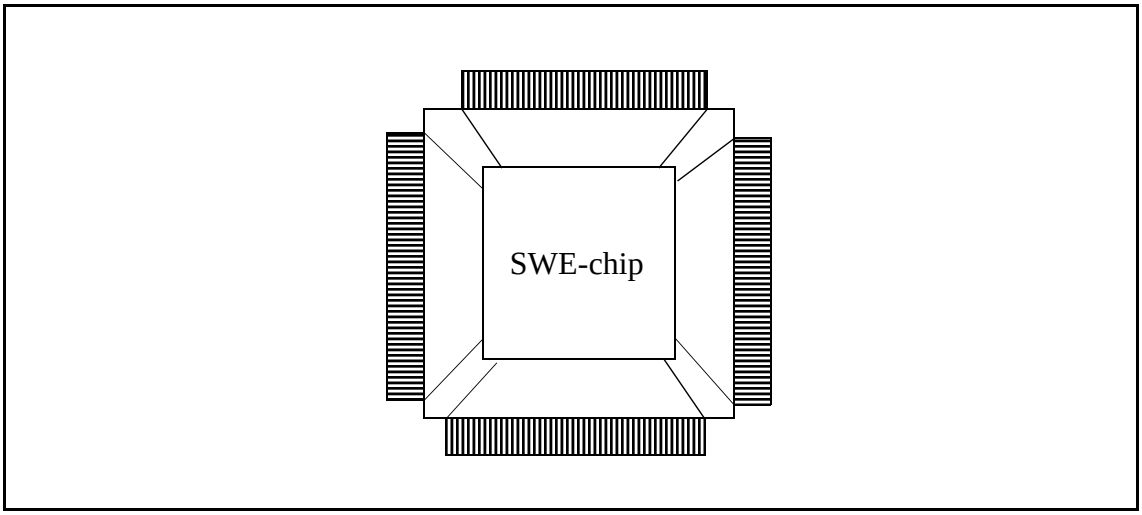

figure 19 The SWE-TAB

TAB PINOUT

The SWE-TAB pinout numbering is shown in figure 20. The component is shown with the active chip side up.

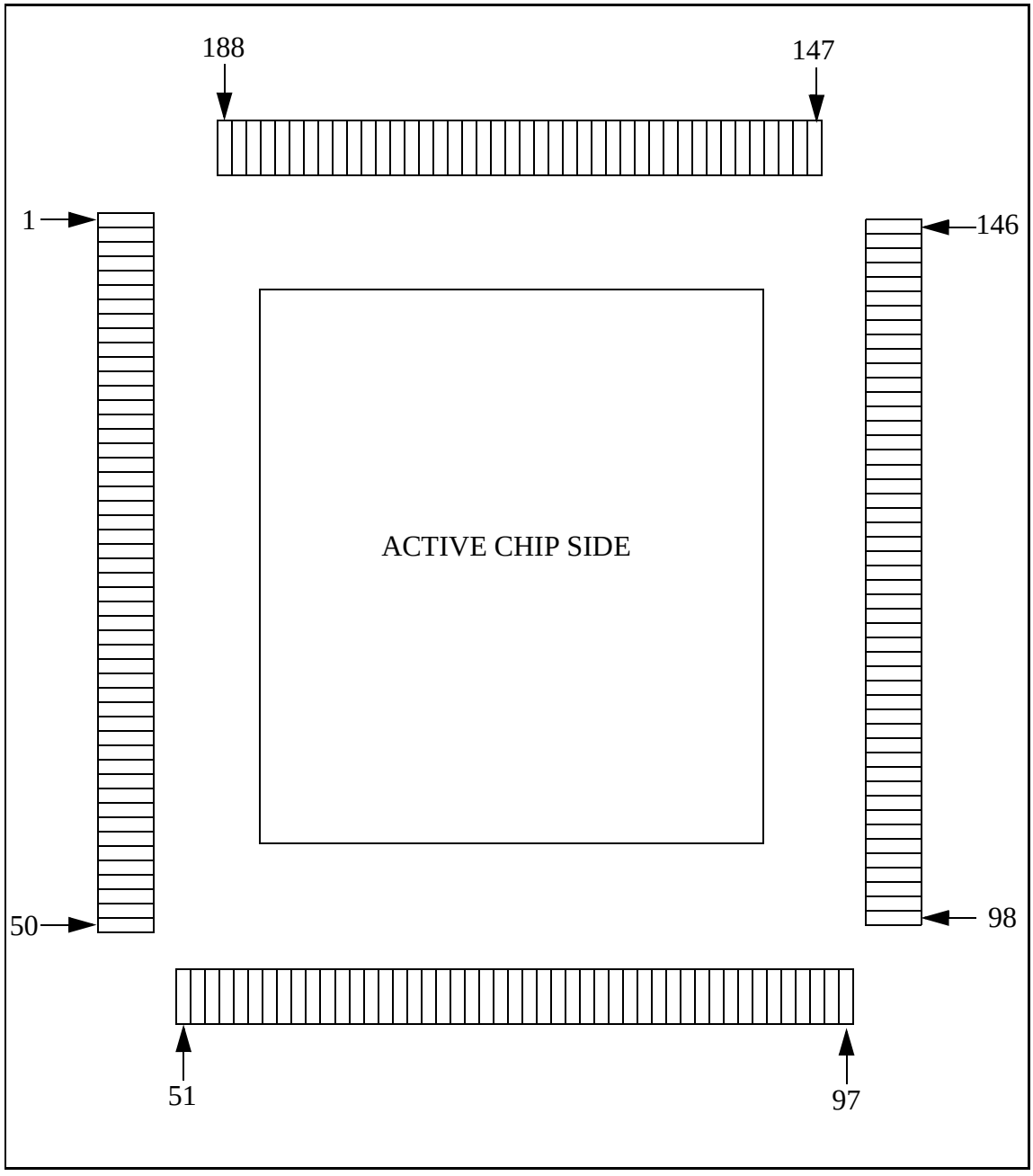

figure 20 SWE-TAB pinout

LEFT

1. +5V	2. SYS_CLK_P	3. SYS_CLK_N
4. +5V	5. SYS_SYNC_P	6. SYS_SYNC_N
7. C_SEL	8. 0V	9. DIN0
10. 0V	11. DIN1	12. DIN2
13. 0V	14. DIN3	15. +5V
16. DIN4	17. DIN5	18. 0V
19. DIN6	20. 0V	21. DIN7
22. DIN8	23. 0V	24. DIN9
25. +5V	26. DIN10	27. DIN11
28. DIN12	29. 0V	30. DIN13
31. 0V	32. DIN14	33. DIN15
34. 0V	35. DIN16	36. +5V
37. DIN17	38. DIN18	39. 0V
40. DIN19	41. 0V	42. DIN20
43. DIN21	44. 0V	45. DIN22
46. +5V	47. DIN23	48. SYN_I
49 0V	50. CL_I	

DOWN

51. D0	52. +5V	53. D1
54. D2	55. 0V	56. D3
57. D4	58. +5V	59. D5
60. D6	61. 0V	62. D7
63. +5V	64. $\overline{\text{DTACK}}$	65. 0V
66. TP0	67. +5V	68. TP1
69. TP2	70. 0V	71. TP3
72. +5V	73. A0	74. A1

75. A2	76. 0V	77. A3
78. A4	79. A5	80. +5V
81. $\overline{RW}$	82. $\overline{DS}$	83. 0V
84. $\overline{CSEL1}$	85. $\overline{CSEL2}$	86. 0V
87. TS0	88. TS1	89. DIV_LSB
90. 0V	91. DIV_MSB	92. TS2
93. TS3	94. +5V	95. TS4
96. 0V	97. TS5	

RIGHT

98. CL_O	99. 0V	100. SYN_O
101. DOUT23	102. +3V	103. DOUT22
104. 0V	105. DOUT21	106. DOUT20
107. +3V	108. DOUT19	109. 0V
110. DOUT18	111. DOUT17	112. +3V
113. DOUT16	114. 0V	115. DOUT15
116. DOUT14	117. +3V	118. DOUT13
119. 0V	120. DOUT12	121. DOUT11
122. DOUT10	123. +3V	124. DOUT9
125. 0V	126. DOUT8	127. DOUT7
128. +3V	129. DOUT6	130. 0V
131. DOUT5	132. DOUT4	133. +3V
134. DOUT3	135. 0V	136. DOUT2
137. DOUT1	138. +3V	139. DOUT0
140. 0V	141. +5V	142. S_SYNC_P
143. S_SYNC_N	144. +5V	145. S_CLK_P
146. S_CLK_N		

UP

147. +5V	148. 0V	149. SDI2_P
150. SDI2_N	151. 0V	152. SI_CLK2_P
153. SI_CLK2_N	154. +5V	155. 0V
156. SDO2_P	157. SDO2_N	158. +5V
159. SO_CLK2_P	160. SO_CLK2_N	161. +5V
162. 0V	163. +5V	164. SDI1_P
165. SDI1_N	166. 0V	167. SI_CLK1_P
168. SI_CLK1_N	169. +5V	170. 0V
171. SDO1_P	172. SDO1_N	173. +5V
174. SO_CLK1_P	175. SO_CLK1_N	176. +5V
177. 0V	178. M_CLK_P	179. M_CLK_N
180. 0V	181. +5V	182. +5V
183. SYS_SY_P	184. SYS_SY_N	185. 0V
186. SYS_CL_P	187. SYS_CL_N	188. +5V