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P3A/FAT PROJECT

CSCB BOARD (1551-ROJ 212 14/1)

TECHNICAL DESCRIPTION

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1 Scope

This document is the Technical Description of the Clock Selection and Connection Board (CSCB) ROJ 212 14/1 for ATM-P3A.
It mainly contains the description of the functions performed by the CSCB. However, since it is not possible to understand the meaning of CSCB functionality without an overview of the complete System Clock Generation, in the next chapter we will briefly describe it.

2 General

In order to make the System Clock Generation operating, three different boards are needed: 2 Clock Boards (CB) and one Clock Selection and Connection Board (CSCB).
The CSCB is devoted to interfacing the 2.048 MHz reference clock with the CB's and to mix the two 155.52 MHz from CB's.
The other interworking regards the lock information from the CB's to the CSCB (Enable signal).
Eventually the two CB's exchange DP's informations each other via RS232 backplane connection.
All the logical connections towards, from and between the boards and the block-diagram of the CSCB are shown in the fig. 1.
The CSCB receives as input the synchronization signals and gives as output the stable clock signal (155.52 MHz). This signal is generated in the CBs using the synchronization signals as reference.
We can achieve a fully duplication by using two different sources at 2.048 MHz and 155.52 MHz as inputs; the former two are available only in the central node and come from the operating company's synchronization network, the latter two are available also in the remote node and come from the ET's clock extraction circuitry (based on an STM-1 data stream).
The 2.048 MHz signals get the CB's through the CSCB, while the 155.52 MHz are straightly connected to the CB's.
One of the two CB is defined as "master" by means of an external hardware connection and/or of DP's command.

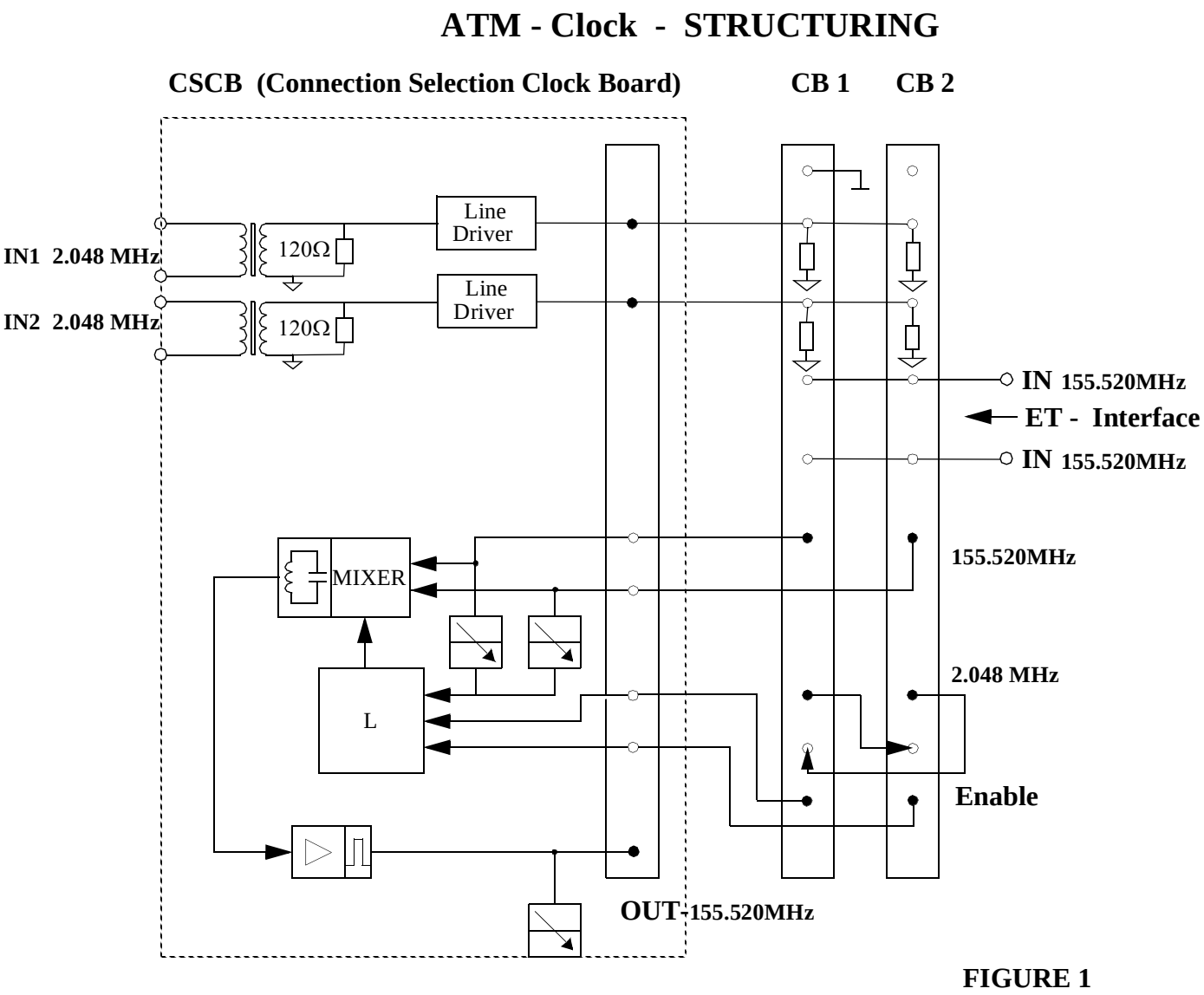

FIGURE 1

3 Interfaces

In CSCB we have the following interfaces:

- INPUT

2 x 2.048 MHz (G. 703)	from Deutch Sync. Network
2 x 155.52 MHz	from the CBs;
2 x Enables	from the CBs;

+5 V	from the CBs;
-5 V	from the CBs;
- OUTPUT	
155.52 MHz	towards the switch;
2 x 2.048 MHz	to be forwarded to CB's.

3.1 Input 2.048 MHz interface

The two inputs 2.048 MHz follow the G. 703 CCITT Recommendation. We receive them on a 120 ohm twisted pair cable plugged at the board front.
We get them through two input transformers for ground separation and impedance matching, make the conversion to C-MOS level and provide them to the CB's.

3.2 Input 155.52 MHz interface

The two 155.52 MHz from the CB's are ECL signals terminated on a 50 ohm pull down resistor to -2 Volt.
We use them to generate the output clock to be distributed towards the switch.

3.3 Input Enable interface

They are TTL level logic signals coming from the CBs. They carry the information about the accuracy of the 155.52 MHz signal received by each CB.

3.4 Output 155.52 MHz interface

The 155.52 MHz clock, is distributed via backplane to the SWM (12 or 24), are pseudo-ECL (+5 Volt supply and 300 ohm pull down resistor to +3 Volt).

3.5 Output 2.048 MHz interface

The two output 2.048 MHz are C-MOS signals.

3.6 Connectors' pin out

The connectors used for the CSCB are:
1> Ethernet Connector (120 ohm) for 2.048 MHz inputs front connection;
2> AMP 2mm Z-Pack HM style A type, RNV 4111121, for all other signals and power feeding. The CSCB has three of them with signals distribution described in the following tables:

CSCB CONNECTOR POSITION 1

AMP 2MM Z-Pack HM Style A

PIN	A	B	C	D	E
01	0	-48	0	-48	0
02	0	-48	0	-48	0
03	0	-48	0	-48	0
04	0	0	0	DP_CSCB	0
05	0	0	0	0	0
06	0	0	0	0	0
07	0	-5_M	0	-5_S	0
08	0	-5_M	0	-5_S	0
09	0	-5_M	0	-5_S	0
10	0	-5_M	0	-5_S	0
11	0	-5_M	0	-5_S	0
12	**FOR CENTERING AND GUIDING**				
13					
14					
15	0		0		0
16	0		0		0
17	0		0		0
18	0		0		0
19	0		0		0
20	0	0	0	0	0
21	0	+5_M	0	+5_M	0
22	0	+5_M	0	+5_M	0
23	0	+5_M	0	+5_M	0
24	0	+5_M	0	+5_M	0
25	0	+5_M	0	+5_M	0

CSCB CONNECTOR POSITION 3

AMP 2MM Z-Pack HM Style A

PIN	A	B	C	D	E
01	0	0	0	0	0
02	0	IN155P1	0		0
03	0	IN155N1	0	0	0
04	0	0	0	IN155N2	0
05	0	0	0	IN155P2	0
06	0		0	0	0
07	0		0		0
08	0		0		0
09	0		0		0
10	0		0		0
11	0	0	0	0	0
12	**FOR CENTERING AND GUIDING**				
13					
14					
15	0	0	0	0	0
16	0	MOUT1	0	MOUT2	0
17	0	0	0	0	0
18	0		0		0
19	0	0	0	0	0
20	0	MIR1_N	0	MIR2_N	0
21	0	MIR1_N	0	MIR2_N	0
22	0	MIT_N	0	ENA1_N	0
23	0	MIT_N	0	ENA2_N	0
24	0	ALIM_N	0		0
25	0		0		0

CSCB CONNECTOR POSITION 5

AMP 2MM Z-Pack HM Style A

PIN	A	B	C	D	E
01	0		0		0
02	0		0		0
03	0		0		0
04	0		0		0
05	0		0		0
06	0	L_CSCB	0		0
07	0	LED	0		0
08	0	SDA	0		0
09	0	WC	0		0
10	0	SCL	0		0
11	0	0	0	0	0
12	**FOR CENTERING AND GUIDING**				
13					
14					
15	0		0		0
16	0		0		0
17	0		0		0
18	0		0		0
19	0		0	0	0
20	0		0	MCLKN	0
21	0		0	MCLKP	0
22	0	0	0	0	0
23	0	-48	0	-48	0
24	0	-48	0	-48	0
25	0	-48	0	-48	0

3.7 Signals description

-48:	auxiliary voltage;
-5_M:	primary voltage -5 Volt from CB1;
-5_S:	primary voltage -5 Volt from CB2;
+5_M:	primary voltage +5 Volt from CB1;
+5_S:	primary voltage +5 Volt from CB2;
DP_CSCB:	CSCB plugging alarm towards CBs;
IN155P1:	155.52 MHz positive pulse input from CB1;
IN155N1:	155.52 MHz negative pulse input from CB1;
IN155N2:	155.52 MHz positive pulse input from CB2;
IN155P2:	155.52 MHz negative pulse input from CB2;
MOUT1:	first 2.048 MHz output;
MOUT2:	second 2.048 MHz output;
MIR_1N:	loss of carrier of 155.52 MHz input from CB1;
MIR_2N:	loss of carrier of 155.52 MHz input from CB2;
MIT_N:	loss of carrier of 155.52 MHz clock output;
ALIM_N:	power feeding alarm;
ENA1_N:	Enable alarm from CB1;
ENA2_N:	Enable alarm from CB2;
L_CSCB:	CSCB LED driver from CBs;
LED:	LED board activation information;
SDA:	EEPROM address interface;
WC:	EEPROM address interface;
SCL:	EEPROM address interface;
MCLKN:	155.52 MHz negative pulse clock output;
MCLKP:	155.52 MHz positive pulse clock output.

4 Functionality

The main CSCB functionality is to distribute the system clock to the switch.
The board receives as input the synchronization signals generated in the two CBs (Clock Board) and gives as output the stable clock signal (155.52 MHz). This is achieved using a circuit that mixes the above mentioned input signals. So the phase of the output clock signal will be the average of the phases of the two input signal. We use this strategy in order to have no interruption in the output signal in case one of the two CBs fails.
Each CB can have two kind of faults:
1> loosing of reference clock which the CB is locked to. In this case the CB quickly switches to the first higher priority avail-

able reference clock signal and locks to it. During this fast operation, there is no interruption of signal transmission from CB to CSCB, so for a while the CSCB will distribute an inaccurate clock. However the recovery time is minimized by the high lock speed of the PLL.
2> detection of degradation of clock accuracy in the 155.52 MHz signal provided to CSCB. In this case the CB sends the signal “Enable” to the CSCB, so it stops mixing the two CB signals and provides the other available CB signal to the output. In this way, when a fault like that is detected, we have no interruption in the CSCB output clock signal but only a little phase change.
Besides the CSCB is also devoted to interfacing the 2.048 MHz reference clock with the CB’s.
Finally we want to highlight the high degree of simplicity and reliability of the CSCB, that it is a very essential requirement for making use of the advantage of CB duplication.

5 Internal structure and hardware blocks

5.1 Internal structure of the core circuit of CSCB

In the previous chapters we described the main functionality and interfaces of the board. We gave also an overview of the complete Synchronization System (see figure1).
Now we want to explain in detail the most important circuit of the CSCB, that is the box called MIXER in figure 1.

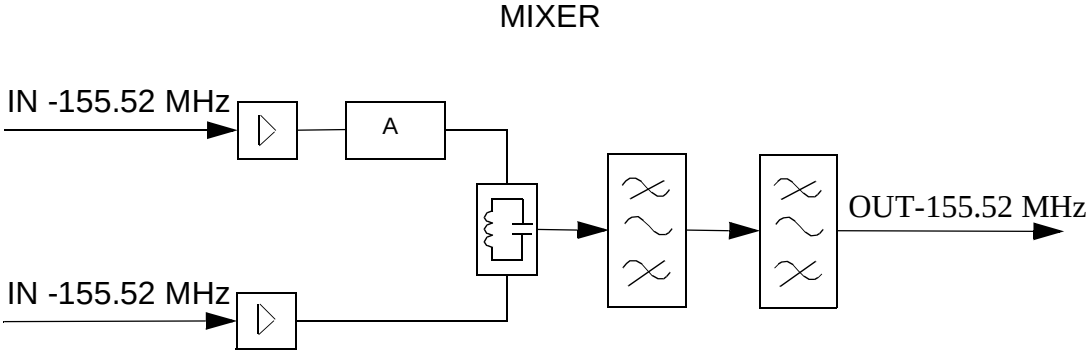

FIGURE 2

First we must clarify that it is not a traditional “mixer”, that is a device

that performs frequency shift of a signal, but we gave it this name because, when the all two input signals are present, it make a mixture of them in order to extracting the output clock. The phase of the achieved output signal is the average of the phases of the two incoming signals.
We have also two band-pass filters to assure the high frequency de-jitteration of the output signal. In future they could be replaced with a SAW-FILTER.
The advantage of this solution in comparison with a normal analog switch is that, in case of absence of one of the two input signals, we have no interruption in clock distribution, but only a little phase shift. That's the reason of our choice.

5.2 Power Block

No DC/DC converters are foreseen, the board receives the +5V and -5V from the CB's in an OR configuration.

The CSCB power consumption is 4 Watt.

5.3 Identification Block

The board can be fully identified thanks to a serial EEprom that can be read by one CB's DP, where the following informations are stored: product identity, revision and serial product number (for further informations see "BOARD ADDRESS AND ALARMS P3A" TH- 93:0045 Uen).
As far as the board is plugged in, a CSB pin and a CB pin are connected each other via backplane; the former is connected to ground, the latter to a pull-up on board. This allows the CB's DP to know if the board is plugged in or not.

6 Test requirements

6.1 Test Facilities

In the CSCB only one test point, needed to read the 155.52 MHz frequency, is foreseen.
We also have a yellow LED, RKZ 93103, for fault signalling.

7 Technical requirements

7.1 Physical Layout

According to layer-drawing described in FAT 10583-1004 Uen

and layer specification 1301-BYC101409 Uen.
Some further details are in layout constrain described in "DESIGN REVIEW MEETING UNITA' CSCB (ATM) ROJ 212 14/1" TH - 93:051 Uit.

7.2 MTBF requirements

The MTBF of CSCB is evaluated around 200 years.

8 Mechanical requirements

See "P3A PROJECT FOR DBP EQUIPMENT PRACTICE" XT/PE - 93:277 Uen.

9 Identification

ROJ 212 14/1.

10 List of open issues

To be written.

11 Abbreviations

CB = Clock board
CSCB = Clock Selection and Connection Board

All the terminology meets the definition in AXE-N words and AXE-N terminology.

VST stands for Central Node;
AEE stands for Remote Node.

12 References

1> "Technical Report, ATM-X Prototype System" (X92-2663) issued by EUA and "Broadband ISDN Pilot Project, OPERATING REQUIREMENTS FOR CONNECTIONS AND TERMINAL EQUIPMENT" issued by DBP Telekom.
2> "ATM - CLOCK" XT/TT- 93:231 Uen.
3> "DESIGN REVIEW MEETING UNITA' CSCB (ATM) ROJ 212 14/1" TH - 93:051 Uit.
4> "P3A PROJECT FOR DBP EQUIPMENT PRACTICE" XT/PE - 93:277 Uen.

5> “BOARD ADDRESS AND ALARMS P3A” TH - 93:0045 Uen
6> “CROSS-SECTION DRAWING” 1301-BYC101409 Uen;
7> “SPECIAL LAYER-DRAWING FOR ATM BOARDS” FAT10583-1004 Uen.