P3A/FAT PROJECT

COB BOARD (1551-ROJ 212 18/1)

TECHNICAL DESCRIPTION

INDEX:

1 Scope

This is the Technical Description relative to the last release of the COB (Communication Board).
It contains the specifications of the functions performed by the above mentioned board, and also informations about timing, mechanics, components, power and alarms.

2 General

As it has been stated in the document of Ref. 1, the Communication Boards are devoted to connect the two cabinets constituting the nodes. In particular the Communication Boards allow the interconnections between the Switch Module (SWM 24/12) and the Switch Ports.
Since the Communication Boards electrically connect the Switch Ports to the Switch Element of the Switch Core in the nodes, the used components and transmission media must make available a frequency of 155.520 Mhz with negligible distorsion and attenuation. According to X 93 0239 and X 93 0295 documents the data and clock signals must be phase-aligned at the input of the Switch Elements and of the Switch Ports.

3 History

P3A/FAT Design Specifications for COB ROJ 212 18/1
Rev. A 1993-07-19 (TH/D-93:064 Uen)

4 Interfaces

As it has been stated in the Implementation Proposal (Ref. 1), the Communication Board has two interfaces, interfacing respectively with the Switch Element and the Transmission Medium. Each interface has a set of data signals and its clock coming in and a set of data signals and its clock coming out of

the Board. The two interfaces will be called Switch Core interface and Transmission Medium interface.

4.1 'Switch Core' interface

4.1.1 Description

The Switch Core interface is constituted by the data signal and its clock coming from the Switch Element and going to the Switch Element. All the signals are balanced differential.

4.1.2 Signals

- Clock input.
This differential PECL input is the 155.52 MHz clock. The clock is supposed to be phase-aligned with the corresponding data input according to Ref. 2.
- Data input.
It is a differential PECL input (the voltage swing is limited to 250 mV).
- Clock output.
This differential PECL input is the 155.52 MHz clock. The clock is phase-aligned with the corresponding data output within the requirements of Ref. 2.
- Data output.
It is a differential PECL output.

4.1.3 Connectors pin out

The Connectors pin out of the 'Switch Core' interface is described in the following Tables.

COB Connector Pos. 1 (900)
AMP 2MM Z-Pack HM Style A RNV 411 1121

Table 1:

PIN	A	B	C	D	E
01	-48 VA	-48 VA	0	-48 VA	-48 VA
02	-48 VA	-48 VA	0	-48 VA	-48 VA
03	-48 VA	-48 VA	0	-48 VA	-48 VA
04	0	COB	0	0	0
05	0	+5VA	0	CK00C_all	0
06	0	+5VB	0	CK01C_all	0
07	0	+3VA	0	CK02C_all	0
08	0	+3VB	0	CK03C_all	0
09	0	WC	0	CK04C_all	0
10	0	SCL	0	CK05C_all	0
11	0	SDA	0	CK06C_all	0
12	FOR CENTERING AND GUIDING				
13					
14					
15	0	EEP_SEL	0	CK07C_all	0
16	0	VREFC	0	CK08C_all	0
17	0	VREFP	0	CK09C_all	0
18	0	0	0	CK10C_all	0
19	0	CDO11N	0	CK11C_all	0
20	0	CDO11P	0	0	0
21	0	0	0	CCLO11N	0
22	0	0	0	CCLO11P	0
23	0	CDI11N	0	0	0
24	0	CDI11P	0	0	0
25	0	0	0	CCLI11N	0

COB Connector Pos. 2 (901)
AMP 2MM Z-Pack HM Style B RNV 412 1121

Table 2:

PIN	A	B	C	D	E
01	0	0	0	CCLI11P	0
02	0	CDO10N	0	0	0
03	0	CDO10P	0	0	0
04	0	0	0	CCLO10N	0
05	0	0	0	CCLO10P	0
06	0	CDI10N	0	0	0
07	0	CDI10P	0	0	0
08	0	0	0	CCLI10N	0
09	0	0	0	CCLI10P	0
10	0	CDO09N	0	0	0
11	0	CDO09P	0	0	0
12	0	0	0	CCLO09N	0
13	0	0	0	CCLO09P	0
14	0	CDI09N	0	0	0
15	0	CDI09P	0	0	0
16	0	0	0	CCLI09N	0
17	0	0	0	CCLI09P	0
18	0	CDO08N	0	0	0
19	0	CDO08P	0	0	0
20	0	0	0	CCLO08N	0
21	0	0	0	CCLO08P	0
22	0	CDI08N	0	0	0
23	0	CDI08P	0	0	0
24	0	0	0	CCLI08N	0
25	0	0	0	CCLI08P	0

COB Connector Pos. 3 (902)
AMP 2MM Z-Pack HM Style A RNV 411 1121

Table 3:

PIN	A	B	C	D	E
01	0	CDO07N	0	0	0
02	0	CDO07P	0	0	0
03	0	0	0	CCLO07N	0
04	0	0	0	CCLO07P	0
05	0	CDI07N	0	0	0
06	0	CDI07P	0	0	0
07	0	0	0	CCLI07N	0
08	0	0	0	CCLI07P	0
09	0	CDO06N	0	0	0
10	0	CDO06P	0	0	0
11	0	0	0	CCLO06N	0
12	FOR CENTERING AND GUIDING				
13					
14					
15	0	0	0	CCLO06P	0
16	0	CDI06N	0	0	0
17	0	CDI06P	0	0	0
18	0	0	0	CCLI06N	0
19	0	0	0	CCLI06P	0
20	0	CDO05N	0	0	0
21	0	CDO05P	0	0	0
22	0	0	0	CCLO05N	0
23	0	0	0	CCLO05P	0
24	0	CDI05N	0	0	0
25	0	CDI05P	0	0	0

COB Connector Pos. 4 (903)
AMP 2MM Z-Pack HM Style B RNV 412 1121

Table 4:

PIN	A	B	C	D	E
01	0	0	0	CCLI05N	0
02	0	0	0	CCLI05P	0
03	0	CDO04N	0	0	0
04	0	CDO04P	0	0	0
05	0	0	0	CCLO04N	0
06	0	0	0	CCLO04P	0
07	0	CDI04N	0	0	0
08	0	CDI04P	0	0	0
09	0	0	0	CCLI04N	0
10	0	0	0	CCLI04P	0
11	0	CDO03N	0	0	0
12	0	CDO03P	0	0	
13	0	0	0	CCLO03N	0
14	0	0	0	CCLO03P	0
15	0	CDI03N	0	0	0
16	0	CDI03P	0	0	0
17	0	0	0	CCLI03N	0
18	0	0	0	CCLI03P	0
19	0	CDO02N	0	0	0
20	0	CDO02P	0	0	0
21	0	0	0	CCLO02N	0
22	0	0	0	CCLO02P	0
23	0	CDI02N	0	0	0
24	0	CDI02P	0	0	0
25	0	0	0	CCLI02N	0

COB Connector Pos. 5 (904)
AMP 2MM Z-Pack HM Style A RNV 411 1121

Table 5:

PIN	A	B	C	D	E
01	0	0	0	CCLI02P	0
02	0	CDO01N	0	0	0
03	0	CDO01P	0	0	0
04	0	0	0	CCLO01N	0
05	0	0	0	CCLO01P	0
06	0	CDI01N	0	0	0
07	0	CDI01P	0	0	0
08	0	0	0	CCLI01N	0
09	0	0	0	CCLI01P	0
10	0	CDO00N	0	0	0
11	0	CDO00P	0	0	0
12	FOR CENTERING AND GUIDING				
13					
14					
15	0	0	0	CCLO00N	0
16	0	0	0	CCLO00P	0
17	0	CDI00N	0	0	0
18	0	CDI00P	0	0	0
19	0	0	0	CCLI00N	0
20	0	LED1M	0	CCLI00P	0
21	0	LED1S	0	0	0
22	0	ALIM_N	0	0	0
23	-48 VA	-48 VA	0	-48 VA	-48 VA
24	-48 VA	-48 VA	0	-48 VA	-48 VA
25	-48 VA	-48 VA	0	-48 VA	-48 VA

4.1.4 Signals description

The signal description follws.

COB=Identification Pin
WC=EEPROM Address Interface
SCL=EEPROM Address Interface
SDA=EEPROM Address Interface
EEP_SEL=EEPROM Selection
CKxC_all=Clock Alarm Signal x
CDOxN=COB Data Out Signal x negative
CDOxP=COB Data Out Signal x positive
CCLOxN=COB Clock Output x negative
CCLOxP=COB Clock Output x positive
CDIxN=COB Data In Signal x negative
CDIxP=COB Data In Signal x positive
LED1M=Switching On from CB Master
LED1S=Switching On from CB Slave
ALIM_N=Power Alarm
+5VA=Test Point relative to the 5VA Power Supply
+5VB=Test Point relative to the 5VB Power Supply
+3VA=Test Point relative to the 3VA Power Supply
+3VB=Test Point relative to the 3VB Power Supply
VREFC=Test Point relative to the Comparator Reference Voltage for the Clock Alarm System
VREFP=Test Point relative to the Comparator Reference Voltage for the Power Alarm System

4.2 Transmission Medium Interface

4.2.1 Description

The Transmission Medium interface is constituted by the data signal and its clock coming from the Switch Port and going to the SWM. In this case all the signals are unbalanced because, as it has been stated in the Implementation Proposal document, an unbalanced Transmission Medium has been chosen.

4.2.2 Signals

- Clock input.
This input is the 155.52 MHz clock.
- Data input.
It is the data signal associated with the clock input.
- Clock output.
This output is the 155.52 MHz clock.
- Data output.
It is the data output associated with the clock output.

4.2.3 Connectors pin out

COAXIAL CONNECTOR RPT 602 1112
Clock and Data Input and Output

Table 6:

POS.	B1A5	A1A5	B1C5	A1C5
910	DI11C	CKI11C	DO11C	CKO11C
911	DI10C	CKI10C	DO10C	CKO10C
912	DI09C	CKI09C	DO09C	CKO09C
913	DI08C	CKI08C	DO08C	CKO08C
914	DI07C	CKI07C	DO07C	CKO07C
915	DI06C	CKI06C	DO06C	CKO06C
916	DI05C	CKI05C	DO05C	CKO05C
917	DI04C	CKI04C	DO04C	CKO04C
918	DI03C	CKI03C	DO03C	CKO03C
919	DI02C	CKI02C	DO02C	CKO02C
920	DI01C	CKI01C	DO01C	CKO01C
921	DI00C	CKI00C	DO00C	CKO00C

Each position of Table 6 stands for a connector. The coaxial connector is shown in figure 1. The shaded areas represent the ground pins.

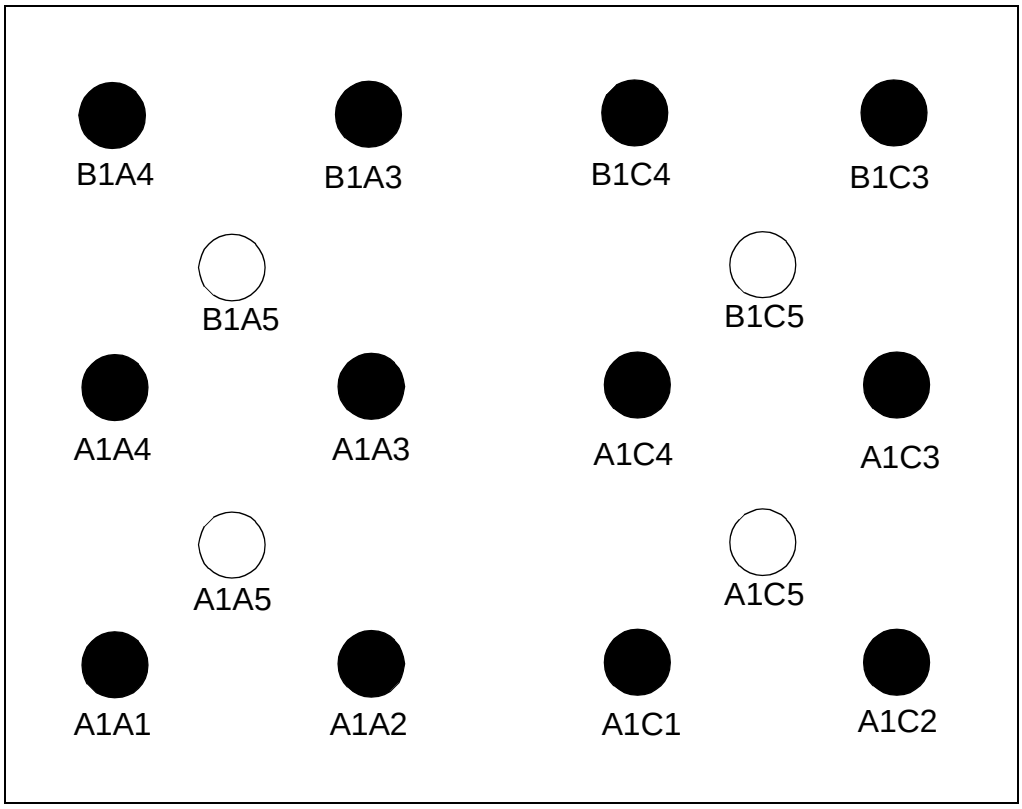

FIG. 1 Coaxial Connector

4.2.4 Signals description

DIxC=Data In x COB
CKIxC=Clock In x COB
DOxC=Data Out x COB
CKOxC= Clock Out c COB

4.3 Power Interface

The Power Module consists of two DC-DC Converters PKE 4211 PI whose output power is 25 W. The two DC-DC Converters power half of the COB respectively so that if there is a failure in one Converter only half of the COB channels are affected.
The Power Module is also in charge of generating the 3V voltage which is necessary for the ECL terminations. This is done thanks to a voltage regulator (See Ref.6).
The Power filter is described in Ref. 3.

4.3.1 Power Consumption

The power consumption of the devices whose power supply is 5 V is about 25W and the power consumption due to the DC-DC Converter efficiency is about 5 W. So the overall COB power consumption is about 30 W.

4.3.2 Signals

The input power signals take the name -48 VA, as it is mentioned in the next sub-chapter.

4.3.3 Connectors/Pinning

See Tables 1 and 5.

5 Functionality

The Communication Board functionality is shown in figure 2.

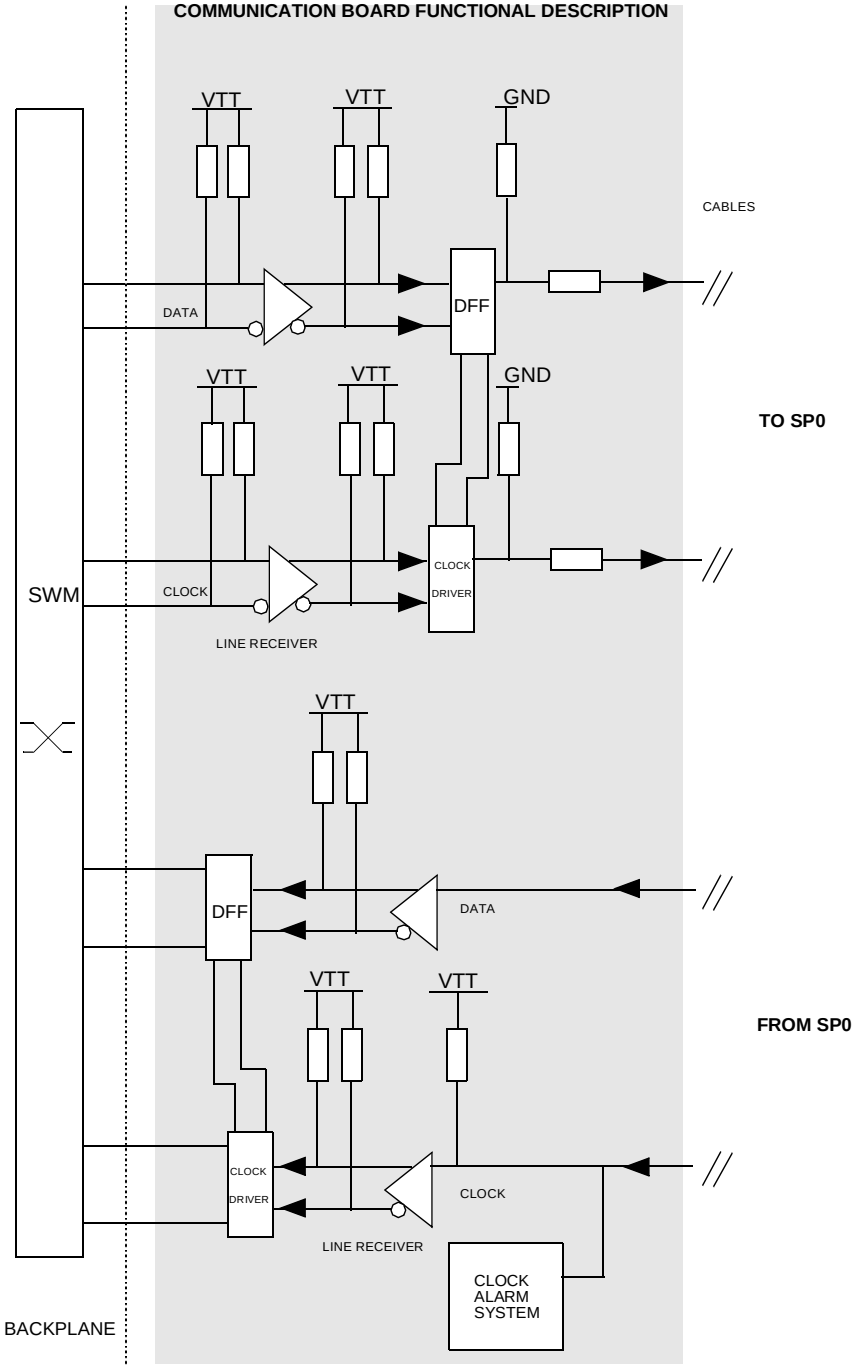
COMMUNICATION BOARD FUNCTIONAL DESCRIPTION
VTT
VTT
GND
CABLES
DATA
DFF
VTT
VTT
GND
TO SP0
SWM
CLOCK
CLOCK
DRIVER
LINE RECEIVER
VTT
DFF
DATA
VTT
VTT
FROM SP0
CLOCK
DRIVER
CLOCK
LINE RECEIVER
CLOCK
ALARM
SYSTEM
BACKPLANE

FIG. 2

As it can be seen from the figure the data, after having been detected, is reclocked both in the transmitting and in the receiving direction.
The transmitted signal reclocking is accomplished because of the phase-differences between the data and the clock which could arise due to the connectors and the stripline characteristic spread on the backplane.
The received data is reclocked after having been detected and before of being transmitted to the Switch Element in order to guarantee the phase-alignment of the data with respect to its clock. In fact such alignment could have been lost because of any delay introduced by the cables.
As it can be seen the interconnection methodology shown in figure 3 refers to an unbalanced connection between the two Communication Boards. The reason for this choice has been explained in Ref. 1.
Then there is a clock alarm system, detecting if the clock is missing. The functional description of figure 2 is relative to one channel. Actually the same functionality is implemented on the Communication Board for twelve channels.

5.1 'Transmitting Reclocking' function

The Reclocking in the Transmitting direction is accomplished by a Line Receiver, a Clock Driver and a DFF in order to align the data and its clock. In fact the data and its clock could have lost their alignment because of the phase differences which can have arisen on the connectors and the stripline characteristic spread on the backplane.

5.2 'Receiving Reclocking' function

The data is reclocked after having been detected and before of being transmitted to the Switch Element in order to guarantee the phase-alignment of the data and the clock which can have been lost because of any delay introduced by the cables.

Also in this case the Reclocking function is accomplished by a Line Receiver, a Clock Driver and a DFF.

5.3 'Clock Alarm' function

The 'Clock Alarm' function is accomplished by the Clock Alarm System of figure 2. An alarm led gets active if the Clock Alarm System detects, by using a peak detector, an incoming clock (available at cables) failure. The associated clock alarm signals are: CKxxC_all.

5.4 'Power Alarm' function

The 'Power Alarm' function is accomplished as the 'Clock Alarm' function. In fact an alarm led gets active if a power failure is detected.

6 Internal structure and HW blocks

As it has been stated there are three HW blocks, each of them corresponding to one of the above mentioned functions, in the Communication Board. The three blocks are named Transmitting Reclocking System, Receiving Reclocking System, Clock Alarm System.

6.1 '*HW block* Transmitting Reclocking System'

The HW block Transmitting Reclocking System consists of a Line Receiver MC100E416, a Clock Driver MC100EL11 and a D Flip-Flop MC100EL52.

6.1.1 *'HW block Transmitting Reclocking'* function

The Line Receiver MC100E416 detects both the signal and its clock coming from the Switch Element. Then the Clock Driver MC100EL11 and the D Flip-Flop MC100EL52 reclock the data

and make available at the output both the reclocked data and the clock.

6.1.2 '*HW block* Transmitting Reclocking' interfaces

- Clock input.
This differential PECL input is the 155.52 MHz clock.
- Data input.
It is a differential PECL input.
- Clock output.
It is an unbalanced 155.52 MHz clock.
- Data output
It is an unbalanced data signal.

6.2 '*HW block* Receiving Reclocking System'

The HW blocks Receiving Reclocking System consists of a Line Receiver MC100E116, a Clock Driver MC100EL11 and a D Flip-Flop MC100EL52.

6.2.1 '*HW block Receiving Reclocking*' function

The Line Receiver MC100E116 detects both the signal and its clock coming from the Switch Port through the cables. Then the Clock Driver MC100EL11 and the D Flip-Flop MC100EL52 reclock the data and make available at the output both the re-clocked data and the clock.

6.2.2 '*HW block Receiving Reclocking*' interfaces

- Clock input.
It is an unbalanced 155.52 MHz clock.
- Data input.
It is an unbalanced data signal.
- Clock output.
This differential PECL output is the 155.52 MHz clock.
- Data output

It is a differential PECL input.

6.3 Identification block

The Board can be fully identified thanks to a serial EEprom that can be read by one CB's DP, where the following informations are stored: product identity, revision and serial product number (for further informations see "BOARD ADDRESS AND ALARMS P3A" TH-93:0045 Uen).
As far as the board is plugged in, a COB pin and a CB pin are connected each other via backplane; the former is connected to ground, the latter to a pull-up on board. This allows the CB's DP to know whether the board is plugged in or not.

7 Alarms and Supervision

As it has been stated above the Communication Board is provided with an Alarm Clock System warning whether the clocks are available from cables or not, and an Alarm Power System warning if the power is missing or not.

8 Test requirements

8.1 Basic Unit Test

See Ref. 7 and Ref. 8.

8.2 Production Test

To be written

8.3 Power Up Test

To be written

8.4 Test Facilities

To be written

9 Technical requirements

9.1 Physical Layout

The Layer drawings are reported in Ref. 4.
The Lay-out constraints are reported in Ref. 5.

9.2 Design requirements

See Reference 1).

9.3 Environmental requirements

To be written

9.4 MTBF requirements

To be written

9.5 EMC requirements

In order to satisfy EMC requirements the following devices have been added.

- Decoupling capacitors between 5V voltage and ground almost for each ECL device.

- Decoupling capacitors between 3V voltage and ground for each termination resistance.

- Clamping diodes at the input of each unbalanced input to protect against electrostatic discharge.

10 Mechanical requirements

The Connectors which are used in the Communication Board are the following.

- AMP 2MM Z-Pack HM Style A (RNV 411 1121)
- AMP 2MM Z-Pack HM Style B (RNV 412 1211)
- Coaxial Connector RPT 602 1112

As from the Implementaion Proposal the Board Size is 265X300 mm.

11 Identification

The COB Identification number is ROJ 212 18/1.

12 References

1) Implementation Proposal for P3A Communication Boards (TH/D-93:055 Uen)

2) ATM-X Switch Port hardware specification (X 93 0295)

3) On Board Power Filtering (TH/A 93:062)

4) XT/PE 93:630 Uen

5) Design Review Meeting COB (TH/A-93:079 Uit)

6) Adjustable Negative Voltage Reference for PECL Circuitry. (TH/D-93:087 Uen)

7) COB But Specifications (TH/D-93:084 Uen)

8) COB But Instructions (TH/D-93:085 Uen)