P3A/FAT PROJECT

CB BOARD (1511-ROJ 212 13/1)

TECHNICAL DESCRIPTION

CONTENTS

1 Scope

This document the Technical Description of the Clock Board (CB) ROJ 212 13/1 for ATM P3A.
It mainly contains the description of the functions performed by the CB. However, since it is not possible to understand the CB functionality without an overview of the complete System Clock Generation, in the next chapter we will briefly describe it.

2 General

In order to make the System Clock Generation operating, three different boards are needed: 2 Clock Boards (CB) and one Clock Selection and Connection Board (CSCB).
The CSCB is devoted to interfacing the 2.048 MHz reference clock with the CB's and to mix the two 155.52 MHz from CB's.
The other interworking regards the lock information from the CB's to the CSCB (Enable signal).
Eventually the two CB's exchange DP's informations each other via RS232 backplane connection.
All the logical connections towards, from and between the boards and the block-diagram of the CSCB are shown in the fig. 1.
The CSCB receives as input the synchronization signals and gives as output the stable clock signal (155.52 MHz). This signal is generated in the CBs using the synchronization signals as reference.
We can achieve a fully duplication by using two CBs driven by two different sources at 2.048 MHz and 155.52 MHz as inputs; the former two are available only in the central node and come from the operating company's synchronization network, the latter two are available also in the remote node and come from the ET's clock extraction circuitry (based on an STM-1 data stream).
The 2.048 MHz signals get the CB's through the CSCB, while the 155.52 MHz are straightly connected to the CB's.
One of the two CB is defined as "master" by means of an external hardware connection and/or of DP's command.

ATM - Clock - STRUCTURING

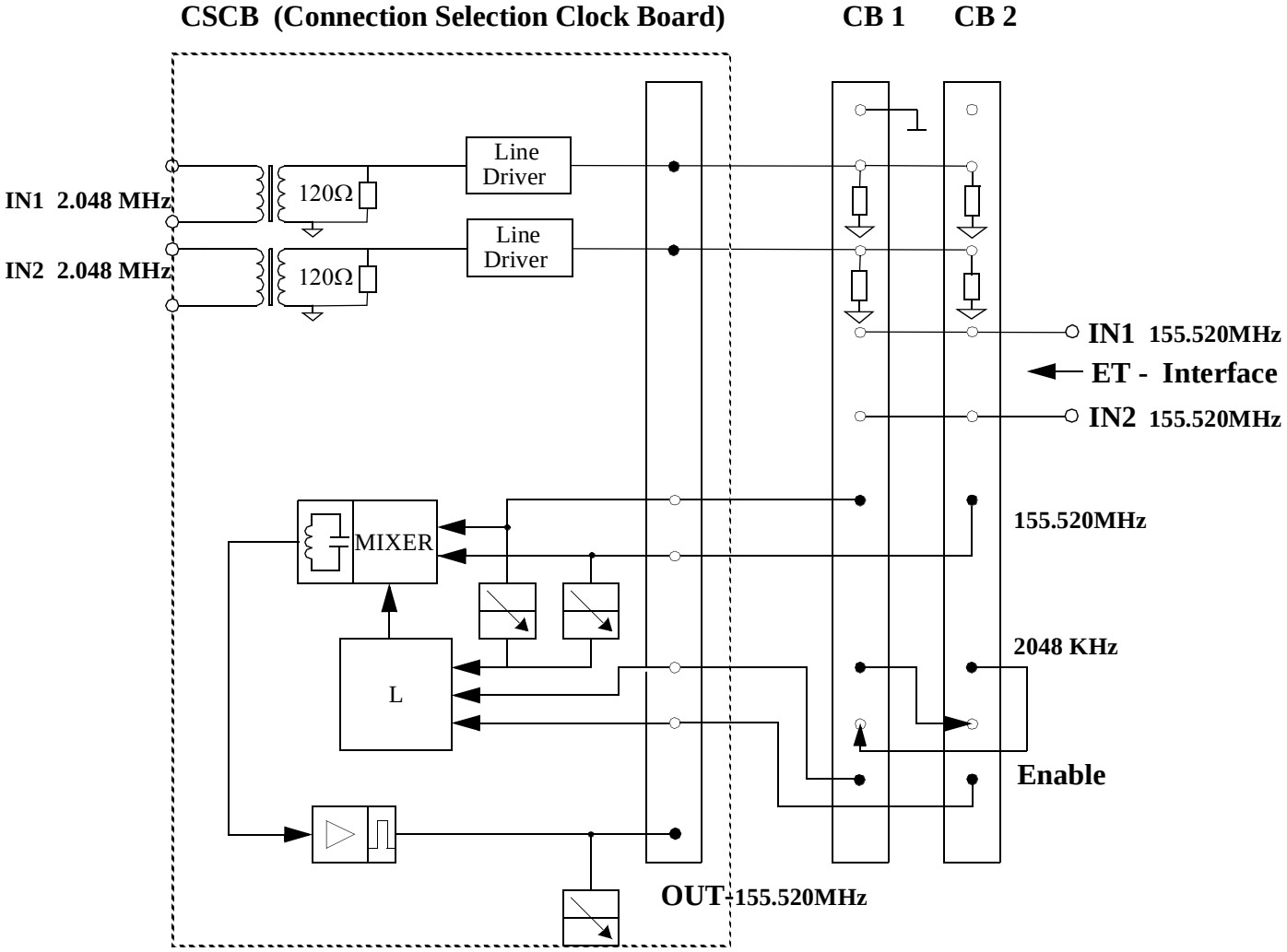


FIGURE 1

3 Interfaces

Each CB features the following interfaces

- INPUT

2 x 2.048 MHz (G. 703)	from the CSCB;
2 x 155.52 MHz	from the ET boards;
1 x 2048 KHz	from the other CB;
2 x -48 Volt	from Power Board;

RS232	for DPs' intercommunication;
RS232	for DP data communication;
ETHERNET	for DP data communication;

- OUTPUT

1 x 155.52 MHz	to the CSCB;
1 x 128 KHz	to the other CSCB;
ENABLE	to the CSCB;
ETHERNET	for DP data communication;
RS232	for DPs' intercommunication;
RS232	for DP data communication.

3.1 Input 2.048 MHz interface

The two input 2.048 MHz are C-MOS signals.

3.2 Input 155.52 MHz interface

The two 155.52 MHz from ET's must be ECL signals to be terminated on the board on 50 ohm pull down resistor to -2 Volt.

3.3 Input 2048 KHz interface

The 2048 KHz is CMOS signal.

3.4 Output 155.52 MHz interface

The 155.52 MHz to the CSCB are ECL signals. They have to be terminated on a 300 ohm pull down resistor to -2 Volt on CSCB.

3.5 Output 2048 KHz interface

The 2048 KHz is a C-MOS signal.

3.6 Output ENABLE interface

Logic TTL signal. It is sent towards the CSCB, carrying the information about the validity of the 155.52 MHz output synchronism signal.

3.7 Connectors' pin out

The connectors used for the CB are:
1> RNV 41501 for the HUB connections.
2> AMP 2 mm Z-Pack HNM style A type RNV 4111121 for all other signals and power feeding. The CB has three of them with signals distribution described in the following tables:

CB CONNECTOR POSITION 1 (900)

AMP 2MM Z-Pack HM Style A

PIN	A	B	C	D	E
01	-48	-48	0	-48	-48
02	-48	-48	0	-48	-48
03	-48	-48	0	-48	-48
04	0	DP_CSCB	0	CK1C_a1	0
05	0	DP_COB1	0	CK2C_a1	0
06	0	DP_COB2	0	CK3C_a1	0
07	0	-5_OUT	0	CK4C_a1	0
08	0	-5_OUT	0	CK5C_a1	0
09	0	-5_OUT	0	CK6C_a1	0
10	0	-5_OUT	0	CK7C_a1	0
11	0	-5_OUT	0	CK8C_a1	0
12	**FOR CENTERING AND GUIDING**				
13					
14					
15	0	CK1C_a2	0	CK9C_a1	0
16	0	CK2C_a2	0	CK10C_a1	0
17	0	CK3C_a2	0	CK11C_a1	0
18	0	CK4C_a2	0	CK12C_a1	0
19	0	CK5C_a2	0	CK6C_a2	0
20	0	MASTER	0	CK7C_a2	0
21	0	+5_OUT	0	CK8C_a2	0
22	0	+5_OUT	0	CK9C_a2	0
23	0	+5_OUT	0	CK10C_a2	0
24	0	+5_OUT	0	CK11C_a2	0
25	0	+5_OUT	0	CK12C_a2	0

CB CONNECTOR POSITION 3 (902)

AMP 2MM Z-Pack HM Style A

PIN	A	B	C	D	E
01	0	0	0	0	0
02	0	0	0	IN1_155P	0
03	0	0	0	IN1_155N	0
04	0	OU_155P	0	0	0
05	0	OU_155N	0	0	0
06	0	0	0	IN2_155P	0
07	0	0	0	IN2_155N	0
08	0	0	0	0	0
09	0	IN2MEX	0	OUT2MEX	0
10	0	0	0	0	0
11	0	0	0	0	0
12	**FOR CENTERING AND GUIDING**				
13					
14					
15	0	0	0	0	0
16	0	M2_IN1	0	M2_IN1	0
17	0	0	07z	0	0
18	0	RX_se_cb	0	TX_se_cb	0
19	0	0	0	0	0
20	0	CK_se_in	0	CK_se_ou	0
21	0	0	0	0	0
22	0	MIR1_N	0	MIR2_N	0
23	0	MIT_N	0	ENA1_N	0
24	0	ALIM_N	0		0
25	0	0	0	0	0

CB CONNECTOR POSITION 5 (904)

AMP 2MM Z-Pack HM Style A

PIN	A	B	C	D	E
01	0		0		0
02	0	RX_SER	0	TX_SER	0
03	0		0	TRIG	0
04	0	RESET	0	TEST	0
05	0	W_EEP	0	L_COB2	0
06	0	L_CSCB	0	L_COB1	0
07	0	LED	0	FANAL1	0
08	0	SDA	0	FANAL2	0
09	0	WC	0	PMAL1	0
10	0	SCL	0	PMAL2	0
11	0	0	0	0	0
12	**FOR CENTERING AND GUIDING**				
13					
14					
15	0	SN7	0	SN8	0
16	0	SN5	0	SN6	0
17	0	SN3	0	SN4	0
18	0	SN1	0	SN2	0
19	0	SLN5	0	SLN6	0
20	0	SLN3	0	SLN4	0
21	0	SLN1	0	SLN2	0
22	0	ALIM_1	0	ALIM_2	0
23	-48	-48	0	-48	-48
24	-48	-48	0	-48	-48
25	-48	-48	0	-48	-48

3.8 Signal description

-48:	primary voltage;
-5_OUT:	secondary voltage -5 Volt towards CSCB;
+5_OUT:	secondary voltage +5Volt towards CSCB;
DP_CSCB:	CSCB plugging alarm;
DP_COB1:	COB1 plugging alarm;
DP_COB2:	COB2 plugging alarm;
MASTER:	Master/Slave board definition;
CK(n)C_a1:	channel (n) clock alarm on COB1 (n=1-12);
CK(n)C_a2:	channel (n) clock alarm on COB2 (n=1-12);
IN1_155P:	first 155.52 MHz input positive pulse;
IN1_155N:	first 155.52 MHz input negative pulse;
IN2_155P:	second 155.52 MHz input positive pulse;
IN2_155N:	second 155.52 MHz input negative pulse;
M2_IN1:	first 2.048 MHz from CSCB;
M2_IN1:	second 2.048 MHz from CSCB;
OU_155P:	155.52 MHz output positive pulse;
OU_155N:	155.52 MHz output negative pulse;
IN2MEX	2048 KHz input from other CB;
OUT2MEX:	2048 KHz output towards other CB;
RX_se_cb:	RS232 interface data input from other CB;
TX_se_cb:	RS232 interface data output towards other CB;
CK_se_in:	RS232 interface clock input from other CB;
CK_se_ou:	RS232 interface clock output towards other CB;
MIR1_N:	loss of carrier of 155.52 MHz input (coming from CB1) in CSCB;
MIR2_N:	loss of carrier of 155.52 MHz input (coming from CB2) in CSCB;
MIT_N:	loss of 155 MHz clock output in CSCB;
ENA(n)_N:	Enable alarm towards CSCB (n=1 or 2);
ALIM_N:	power supply alarm in CSCB;
RX_SER:	RS232 input for data communication;
TX:_SER:	RS232 output for data communication;
TRIG:	it is a DP output that can be used to help the trouble-shooting routines
RESET:	it is the DP reset;
TEST:	it is a DP input used to select the DP test mode at power on;
W_EEP:	Write EEPROM;
L_CSCB:	LED driver for CSCB;
L_COB1:	LED driver for COB1;
L_COB2:	LED driver for COB2;
LED:	LED board activation information;
SDA:	EEPROM address interface;
WC:	EEPROM address interface;
SCL:	EEPROM address interface;
FANAL1:	FAN ALarm from SDB;

FANAL2: FAN ALarm from SFB;
PMAL1: power feeding alarm from SDB;
PMAL2: power feeding alarm from SFB;
SN(n): Subrack Number information (n=1-8);
SLN(n): SLot Number information (n=1-8);
ALIM_1: power supply alarm from COB1;
ALIM_2: power supply alarm from COB2.

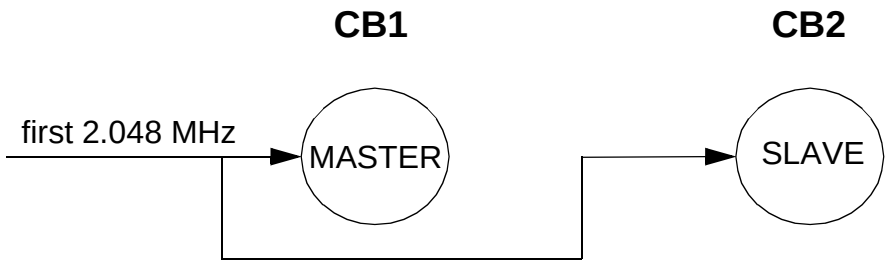
4 Functionality

The board description can be done using the block diagram of figure 2 as reference.
The two CB's are completely identical. There is a backplane pin grounded (MASTER) which needs to make out the master from the slave board; so the master board position is uniquely identified.
The input frequencies needed to build up the clock generating systems are those listed below; each signal comes with a priority level set up by the DP in order to make the board work with the correct input signal.
- The two 2.048 MHz have the highest priority. Even if all the input clocks were available (in the VST node), the CB would synchronize itself to the first 2.048 MHz. Should the first clock fail, the board would switch automatically to the second one.
The selection of which of two clocks comes first is according to the pin numbering.
- The two 155.52 MHz have a lower priority. They are chosen when the two 2.048 MHz are not available (in the AEE node). The selection of which 155.52 MHz is to choose follows the above mentioned criteria.
- The 2048 KHz is an internal signal between CB's. They exchange each other this clock signal, which comes directly by the internal local oscillators (TCXO), with its internal stability, when all the external references fail or are not available.

Eventually the priority is the following:

<1>	2.048 MHz (a)	for both the CB's;
<2>	2.048 MHz (b)	for both the CB's;
<3>	155.52 MHz (a)	for both the CB's;
<4>	155.52 MHz (b)	for both the CB's;
<5>	20.48 MHz from TCXO	for the master board
	2048 KHz from the other CB	for the slave board.

The flow chart describes the master-slave policy.

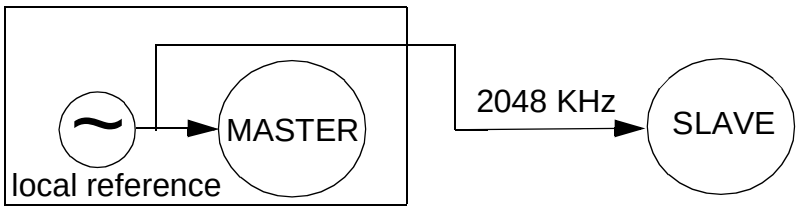


<first 2MHz fails>

<second 2MHz fails>

<first 155MHz fails>

<second 155MHz fails>



<master internal reference fails>

For each input signal a peak detector is foreseen to detect a loss of signal occurrence. The phase detectors play the role to compare the reference clock and the local oscillator replica phases. The frequency to be compared are taken to a suitable value achieved with the minimum even ratio of division; the 2.048 MHz is compared with a 128 KHz. This means that a division by 16 is needed for the 2.048 MHz and one by 1215 for the 155.52 MHz output. The external 155.52 MHz is divided by 36 to get 4.32 MHz.
Instead the 20.48 MHz local oscillator is divided by 160 to be compared with a 128 KHz.
This is an important point because the higher is the ratio the worst the phase comparator works because of jitter increase.
Anyway the Low Pass filter plays a de-jittering role thanks to its narrow bandwidth.
The Low Pass filters make available at their outputs a quasi-DC voltage level (at the operating PLL path it is an actual DC voltage) which get through a selector: this is driven by a supervision logic which tells it what path must be active. A broader Low Pass filter (10 KHz) follows the selector to filter out added noise.
The voltage superimposed to the 155.52 MHz oscillator is sent to a Device Processor through an Analog to Digital Converter. This is for monitoring and supervision long time variations.
If a short time variation occurs, an hardware unlock detector quickly recognizes the fault and transmits an interrupt to DP. The faults and alarms managing is described forward.
The TCXO becomes active as reference every time the master and the slave boards are not provided with the 2.048 MHz and 155.52 MHz signals (for any reason).
The PLL closes itself onto the TCXO achieving its same stability (see for reference the enclosed data sheet).
The voltage feedback by the TCXO drives the oscillator to keep it locked; the DC voltage is also read by DP which switches on an alarm every time the voltage value falls outside a pre determined range.
The oscillator frequency is set by a quartz with a frequency resonance at 25.92 MHz; the output will be got by tuning the sixth harmonic.
At the start up the outputs (155.52 and 4.32 MHz) are kept shut down for around 500 msec, in order to avoid the sending of a not well controlled frequency.

CLOCK BOARD BLOCK DIAGRAM

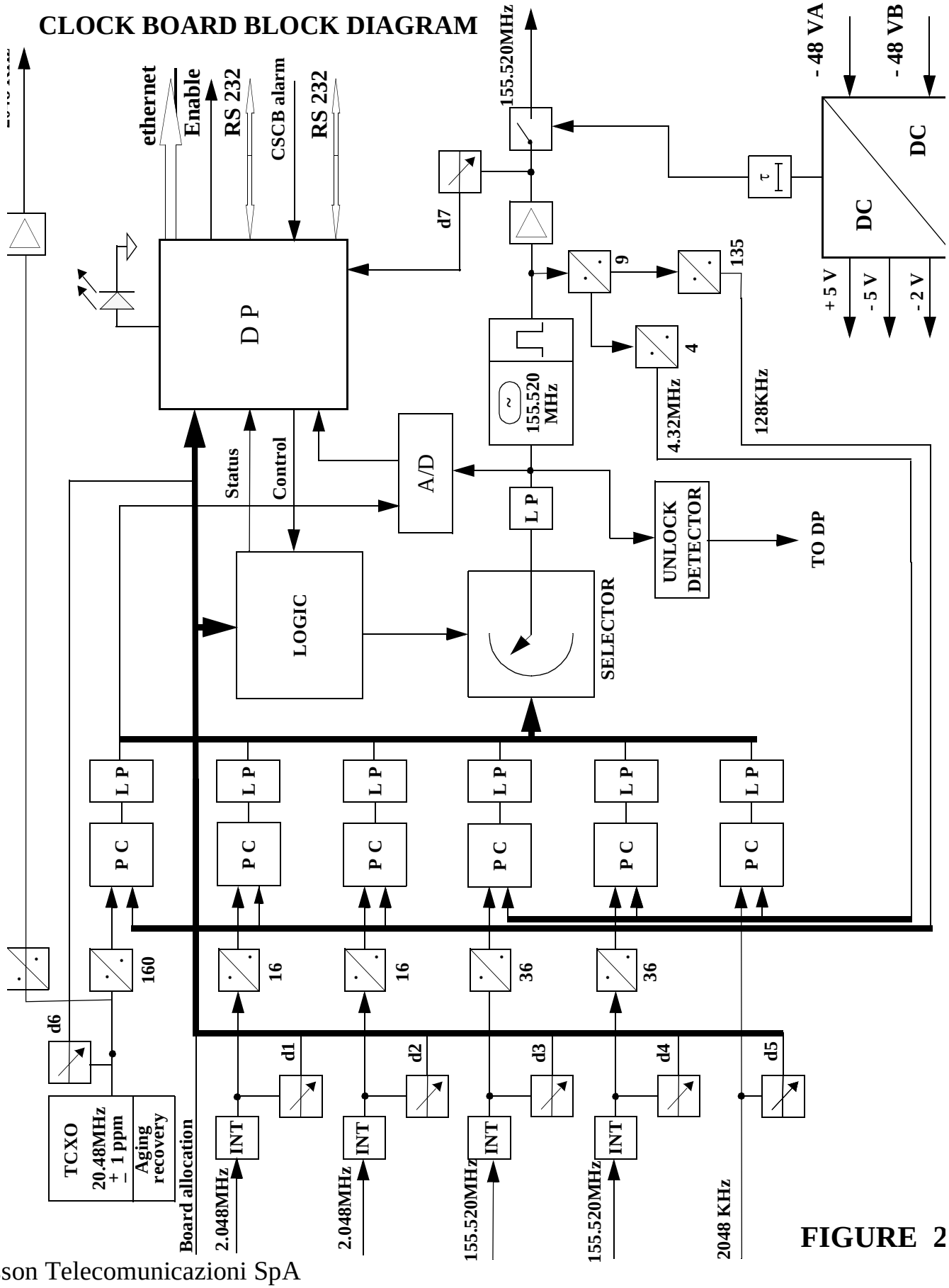


FIGURE 2

5 Internal structure and HW blocks

5.1 Control and supervision block

As described in figure 3, the CB is equipped with a Device Processor Motorola 68302, 64 Kbyte memory, connected through a serial interface to a RS232 connector and through another serial interface to the other CB via backplane.The following device are also connected via bus: a chip set which plays the role of interfacing towards ETHERNET, a ROM 28F001 of 512 Kbyte, a RAM 628512 of 1 Mbyte and to the analog/digital converter.
The DPs, together with some other analog devices, perform the alarms and faults managing, briefly described below.
Further details can be found in "DP SW Specification on CB Board" TH 93:0071 rev. PA1 by Grilli.

Fault at input signals: *Loss_of_input_clock* (1-5).

- HW action:
the peak detectors transmit to the DP the presence or loss of incoming signals and the logic quickly switches to the highest priority available signal.

- SW action:
supervision of logic actions. Check that the same reference is available in the two CBs by using RS232 interface. If one CB cannot detect a reference, which is detected in the other one, the board is pointed as faulty and the Disable signal is sent to CSCB. It is a very important check, because if we two CBs are not locked to the same reference clock, the CSCB could not work correctly. However it is a very low probability fault.

Fault at internal signals: *Loss_of_local_clock*.

- HW action:
the peak detector transmits to the DP the presence or loss of the TCXO.

- SW action:
when this alarm raises the board is pointed as faulty and cannot be master board when the external reference clocks are not available.

Fault at output signals: *Loss_of_155_output.*

- HW action:
the peak detector transmits to the DP the presence or loss of the 155.52 MHz output.

- SW action:
the board is pointed as faulty and must be replaced.

Fault at phase lock: *OUT_ of_lock_warning*.

- HW action:
the DP read via the Analog/Digital converter the actual value of the DC voltage driving the VCXO.
Every time it lies out of the range 1.5 - 3.5, the alarm raises.

- SW action:
the DP, which receives the fault alarm, sends the Disable signal to the CSCB and the board is pointed as faulty.

Fault at phase lock: *Out_of_lock*.

- HW action:
the *unlock detector* sends an alarm to DP.

- SW action:
the DP, which receives the fault alarm, sends the Disable signal to the CSCB and the board is pointed out as faulty.

Board Removal: *Board_removal*.

- HW action:
when a CB is removed, the other CB's DP knows that.

- SW action:
the remaining CB is the only clock source.

Fault on the CSCB: *CSCB_alarm*.

- HW action:
a peak detector reveals the presence or loss of the outgoing clock.

- SW action:
the clock distribution fails.

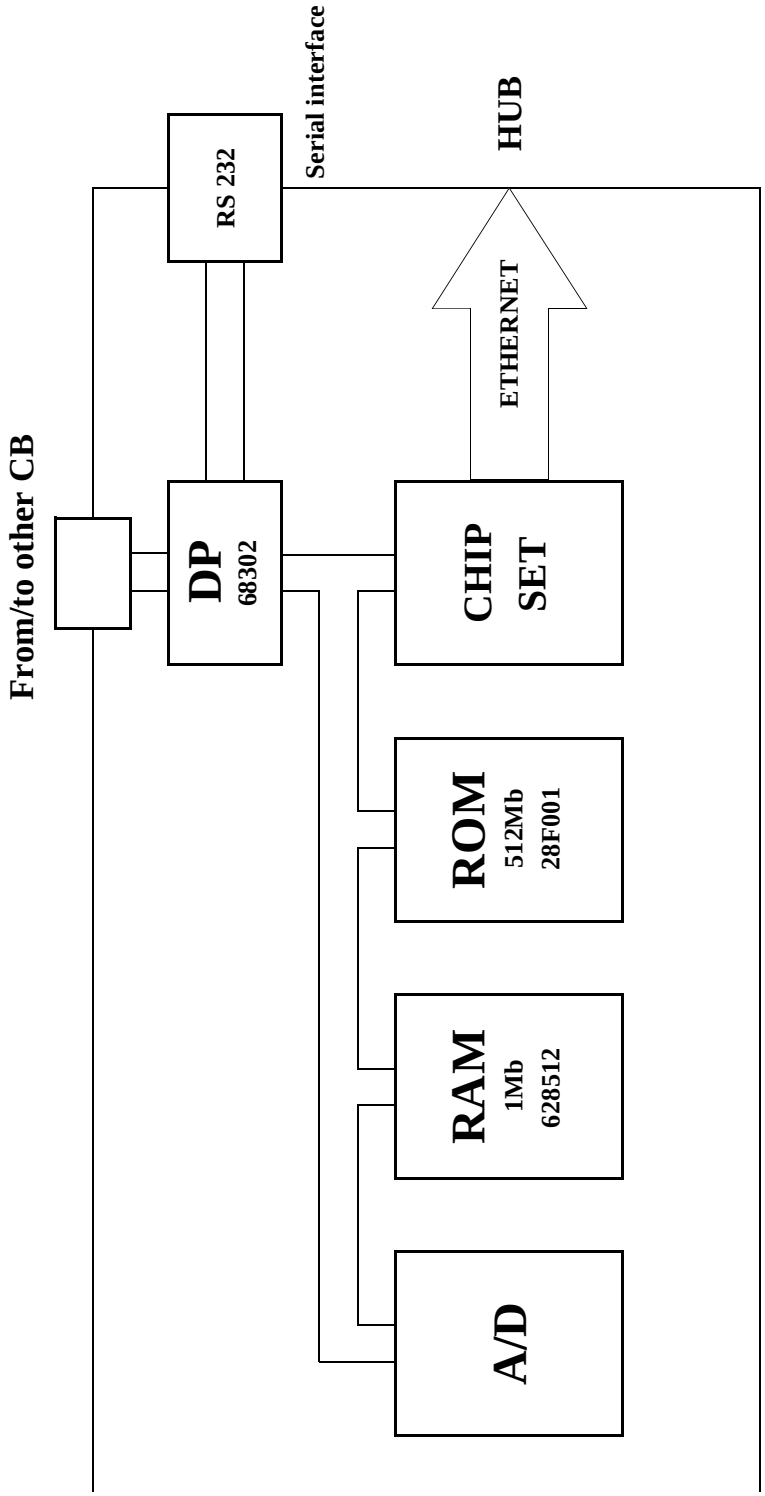
Power fault: *Under_voltage_alarm*.

- HW action:
the voltage levels from DC/DC converters are checked.

- SW action:
the board can not be master.

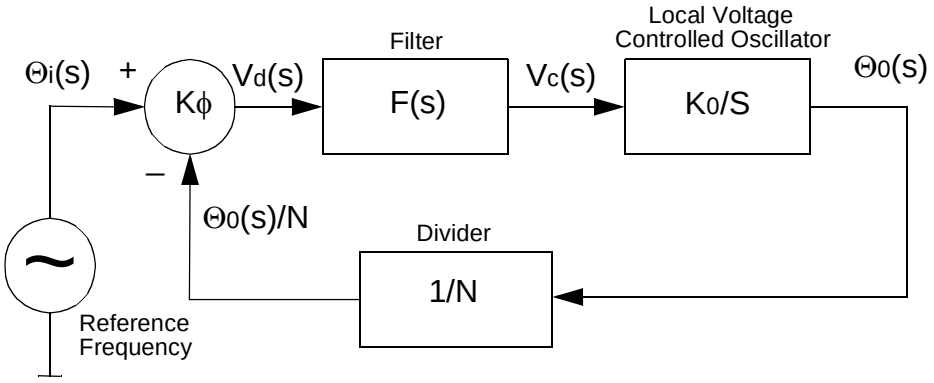
TCXO aging: this alarm is reported to DP.

DP CIRCUIT ON CLOCK BOARD



5.2 PLL and oscillator block

The main Phase Locked Loop characteristics are analyzed in the following.



where:

$$\begin{cases} V_d(s) = K\phi(\Theta_i - \Theta_0) \\ V_c(s) = F(s) * V_d(s) \\ \Theta_0(s) = K_0 * Vc(s) / S \end{cases}$$

$$\Downarrow$$

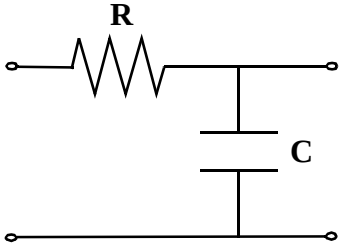
$$\frac{\Theta_0(s)}{\Theta_i(s)} = \frac{K_0 * K\phi * F(s)}{S + K_0 * K\phi * F(s) / N}$$

Closed loop transfer function

A second order PLL with the loop filter described below has been chosen. The loop filter F(s) is:

$$F(s) = \frac{1}{1 + s\tau}$$

referring to the schematic:



$\tau = R\,C$

The F(s) can be re-written:

$$F(s) = \frac{\omega_n^2 \, N}{S^2 + 2 \xi \omega_n S + \omega_n^2}$$

$$\begin{cases} \omega_n = \sqrt{\dfrac{K_\phi K_0}{N \tau}} \\ \xi = \dfrac{1}{2 \tau \omega_n} \end{cases}$$

Another equation derived from the PLL sketch is useful to evaluate the effect of noise $\mathbf{e}_N$ within the VCO driver voltage ε:

$$\frac{\varepsilon}{e_N} = \frac{S^2}{S^2 + 2 \xi \omega_n S + \omega_n^2}$$

It is important because it permits to highlight that, besides lock time and loop filter stability, the value of ξ affects the error reduction output too. So a good trade-off between the loop filter stability and an acceptable error suppression is obtained choosing ξ in the range 0.5 - 0.9.
The phase comparator features a phase gain equal to 0.80 Volt/rad ($\Delta V/2\pi$).
The VCO gain must be estimated by measurements:

$$K_0 = 2 \pi f_0 \frac{\Delta f / f_0}{\Delta V}$$

A list of the main parameters follows:

$\tau = R C$

K_ϕ = phase gain = $0.80 \ \frac{V}{rad}$

K_0 = VCO gain = $12.215 * 10^3 \ \frac{rad}{V S}$

N1 = 1215 (2 MHz reference clock loop)

N2 = 36 (155 MHz or 20.48 MHz reference clock loop)

Choosing: $\xi = 0.8$, we achieve the following values:

R = 485 KΩ C = 100 nFarad in case N = 1215;
R = 14 KΩ C = 100 nFarad in case N = 36.

The oscillator follows a Pierce configuration, using a Quartz whose resonating frequency is 25.92 MHz: the tuning occurs at the sixth harmonic which is exactly 155.52 MHz. As a tuning diode, a Varactor type is used in such an arrangement that a trackability of +/- 25 ppm is achievable within a 0.5 - 4.5 Volt range of DC driving voltage.
The oscillator output is squared and divided properly to get the different frequencies to be compared with the external references. Eventually the 155.52 MHz is distributed through the equipment.
The TCXO, which drives the board in master mode as a local reference, features the following characteristics:
the frequency vs. temperature curve, the supply variations and aging don't give a total deviation larger than 4.6 ppm at a fixed voltage over one month and within the entire life-time of twenty years; the aging of the oscillator after twenty years must not be larger than what is needed to guarantee a maximum total deviation range of 15 ppm with all deviations and at a fixed voltage.

5.3 Power block

The two CBs have three couple of DC/DC converters that convert the primary voltage supply -48 V into three secondary voltages. The concept of duplication has been used in the feeding device too for increasing the system endurance.
The secondary voltages generated in the CBs are provided to CSCB that receives them in a OR configuration.
The circuit used for power filtering is described in "ON BOARD POWER FILTERING" TH/A-93:082 Uen.

The list of the internal voltages needed to the CSCB and CB is:

+5 V for standard logic;
-5 V for ECL logic;
-2 V for ECL terminations.

The CB power consumption is 15 Watt.

5.4 Identification block

The board can be fully identified thanks to a serial EEprom that can be read by one CB's DP, where the following informations are stored: product identity, revision and serial product number (for further informations see "BOARD ADDRESS AND ALARMS P3A" TH- 93:0045 Uen).
As far as the board is plugged in, two CB's pins are connected each other via backplane; the former is connected to ground, the latter to a pull-up on board. This allows the CB's DP to know if the board is plugged in or not.

6 Test requirements

6.1 Basic Unit Test

To be written.

6.2 Production Test

To be written.

6.3 Power Up Test

To be written.

6.4 Test Facilities

In the CB, two measurement points are foreseen: one is needed to get the DC voltage value superimposed to VCXO and another to measure the clock frequency 155.52 MHz.
Besides one yellow LED, RKZ 93103, is foreseen for fault signaling.

7 Technical requirements

7.1 Physical Layout

According to layer-drawing described in FAT 10583-1004 Uen and layer specification 1301-BYC101409 Uen.

7.2 Design requirements

To be written.

7.3 Environmental requirements

To be written.

7.4 MTBF requirements

To be written.

7.5 Requirements to other units

To be written.

8 Mechanical requirements

See “P3A PROJECT FOR DBP EQUIPMENT PRACTICE” XT/PE - 93:277 Uen.

9 Identification

The identification number of this board is ROJ 212 13/1

10 List of open issues

DPs’ actions to be defined in detail.

11 Abbreviations

CB = Clock board
CSCB = Clock Selection and Connection Board

All the terminology meets the definition in AXE-N words and AXE-N terminology.

VST stands for Central Node;
AEE stands for Remote Node.

12 References

1> “Technical Report, ATM-X Prototype System” (X92-2663) issued by EUA and “Broadband ISDN Pilot Project, OPERATING REQUIREMENTS FOR CONNECTIONS AND TERMINAL EQUIPMENT” issued by DBP Telekom.
2> “ATM - CLOCK” XT/TT- 93:231 Uen.
3> “P3A PROJECT FOR DBP EQUIPMENT PRACTICE” XTPE - 93:277 Uen.
4> “BOARD ADDRESS AND ALARMS P3A” TH - 93:0045

Uen

5> “DESIGN SPECIFICATION FOR CSCB ROJ 212 14/1 (P3A PROJECT)” TH/A-93:080 Uen.

6> “CROSS-SECTION DRAWING” 1301-BYC101409 Uen;

7> “SPECIAL LAYER-DRAWING FOR ATM BOARDS” FAT10583-1004 Uen.

8> “ON BOARD POWER FILTERING” TH/A-93:082 Uen.